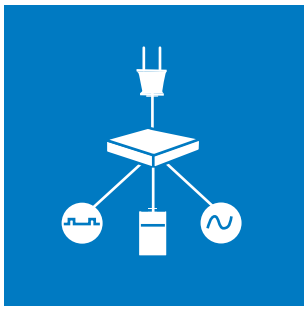

POWER MANAGEMENT

Supervisors

IMP690A,692A, 802L/M, 805L

µP Supervisor with Battery Backup Switch

IMP705/6/7/8, 813L

Low-Power µP Supervisor Circuits

IMP809, IMP810

3-Pin Microcontroller Power Supply Supervisor

IMP811, IMP812

4-Pin µP Voltage Supervisor with Manual Reset

ISO 9001 Registered

408-432-9100/www.impweb.com

Each Part Number Has a Hyper Link To The Data Sheet

Product Selection Guide

Part Number	Backup Battery Switch	Watchdog Timer	Power Fail Comparator Monitor	Manual Reset Pin	Active LOW Reset	Active HIGH Reset	Nominal Threshold Voltage (V)	Maximum Supply Current* (µA)	Packages
IMP690A	X	X	X		X		4.65	100	④, ⑤
IMP692A	X	X	X		X		4.40	100	④, ⑤
IMP705		X	X	X	X		4.65	140	①, ④, ⑤
IMP706		X	X	X	X		4.40	140	①, ④, ⑤
IMP707			X	X	X	X	4.65	140	①, ④, ⑤
IMP708			X	X	X	X	4.40	140	①, ④, ⑤
IMP802L	X	X	X		X		4.65	100	④, ⑤
IMP802M	X	X	X		X		4.40	100	④, ⑤
IMP805L	X	X	X			X	4.40	100	④, ⑤
IMP809J					X		4.00	15	③
IMP809L					X		4.63	15	③
IMP809M					X		4.38	15	③
IMP809R					X		2.63	10	③
IMP809S					X		2.93	10	③
IMP809T					X		3.08	10	③
IMP810J						X	4.00	15	③
IMP810L						X	4.63	15	③
IMP810M						X	4.38	15	③
IMP810R						X	2.63	10	③
IMP810S						X	2.93	10	③
IMP810T						X	3.08	10	③
IMP811J				X	X		4.00	15	②
IMP811L				X	X		4.63	15	②
IMP811M				X	X		4.38	15	②
IMP811R				X	X		2.63	10	②
IMP811S				X	X		2.93	10	②
IMP811T				X	X		3.08	10	②
IMP812J				X		X	4.00	15	②
IMP812L				X		X	4.63	15	②
IMP812M				X		X	4.38	15	②
IMP812R				X		X	2.63	10	②
IMP812S				X		X	2.93	10	②
IMP812T				X		X	3.08	10	②
IMP813L		X	X	X		X	4.65	140	①, ④, ⑤

** Over Operating Temperature Range*

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Packages: ① *8-pin MicroSO*
② *4-pin SOT-143*
③ *3-pin SOT-23*
④ *8-pin Plastic DIP*
⑤ *8-pin SO*

Each Part Number Has a Hyper Link To The Data Sheet

µP Supervisor with Battery Backup Switch

The IMP690A/IMP692A/IMP802L/IMP802M/IMP805L simplify power supply monitoring and control in microprocessor systems. Each circuit implements four functions: Reset control, watchdog monitoring, battery-backup switching and power-failure monitoring. In addition to microprocessor reset under powerup and power-down conditions, these devices provide battery-backup switching to maintain control in power-loss and brown-out situations. Additional monitoring capabilities can provide an early warning of unregulated power-supply loss before the voltage regulator drops out. The important features of these four functions are:

a) 1.6 second watchdog timer to keep microprocessor responsive

b) 4.40V or 4.65V V_{CC} threshold for microprocessor reset at power-up and power-down

c) SPDT (single-pole, double-throw) PMOS switch connects backup power to RAM if V_{CC} fails

d) 1.25V threshold detector for power loss or general purpose voltage monitoring

While these features are pin–compatible with the industry standard power–supply supervisors offered by Maxim, the IMP devices are superior replacements and can reduce power requirements by 70 percent when compared to Maxim MAX690/MAX692A/MAX802L/MAX802M/MAX805L devices. Short-circuit and thermal protection have also been added.

The IMP690A/IMP802L/IMP805L generate a reset pulse when the supply voltage drops below 4.65V, and the IMP692A/IMP802M generate a reset below 4.40V. The IMP802L/IMP802M have power–fail accuracy to ±2%. The IMP805L is the same as the IMP690A except that RESET is provided instead of $\overline{\text{RESET}}$.

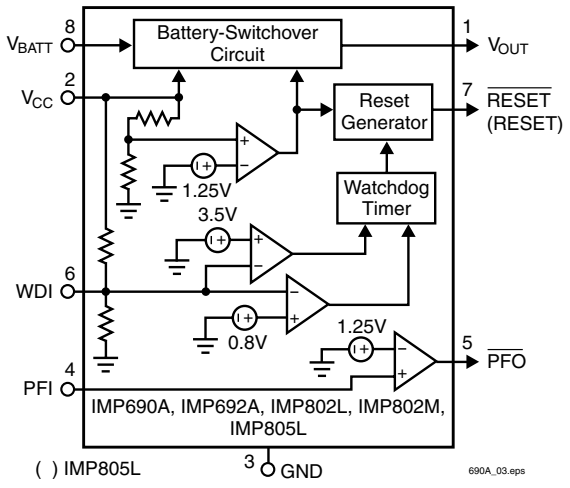
Key Features

- Design improvement over Maxim MAX690A/692A/802L/802M/805L
  - 70% lower current than Maxim: 100µA maximum
  - RESET Operation to 1.1V
- Two precision supply-voltage monitor options
  - 4.65V (IMP690A/802L/805L)
  - 4.40V (IMP692A/802M)
- Battery-backup power switch on-chip
- Watchdog timer: 1.6 second timeout
- Power failure/low battery detection
- Short-circuit protection and thermal limiting
- Small 8-pin SO package
- No external components
- Specified over full temperature range

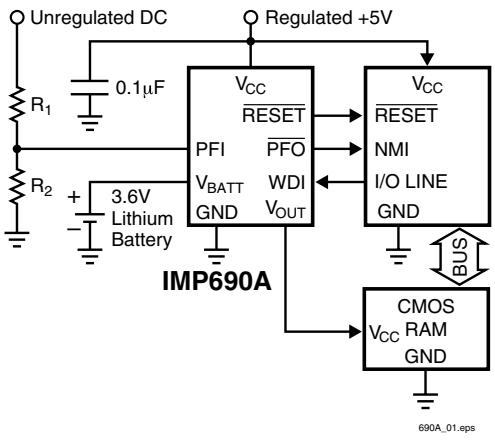
Applications

- Embedded control systems
- Battery–operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment
- µP/µC power supply monitoring

Block Diagrams

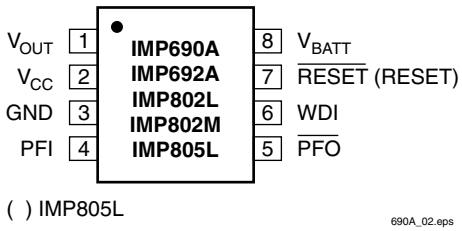


Typical Application



Pin Configuration

Plastic/CerDip/SO



( ) IMP805L

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Ordering Information

Part Number	Reset Threshold (V)	Temperature Range	Pins-Package
IMP690A			
IMP690ACPA	4.5 to 4.75	0°C to +70°C	8-Plastic DIP
IMP690ACSA	4.5 to 4.75	0°C to +70°C	8-SO
IMP690AC/D	4.5 to 4.75	25°C	DICE
IMP690AEPA	4.5 to 4.75	–40°C to +85°C	8-Plastic DIP
IMP690AESA	4.5 to 4.75	–40°C to +85°C	8-SO
IMP690AMJA	4.5 to 4.75	Contact Factory	8-CerDIP
IMP692A			
IMP692ACPA	4.25 to 4.50	0°C to +70°C	8-Plastic DIP
IMP692ACSA	4.25 to 4.50	0°C to +70°C	8-SO
IMP692AC/D	4.25 to 4.50	25°C	DICE
IMP692AEPA	4.25 to 4.50	–40°C to +85°C	8-Plastic DIP
IMP692AESA	4.25 to 4.50	–40°C to +85°C	8-SO
IMP692AMJA	4.25 to 4.50	Contact Factory	8-CerDIP
IMP802L			
IMP802LCPA	4.5 to 4.75	0°C to +70°C	8-Plastic DIP
IMP802LCSA	4.5 to 4.75	0°C to +70°C	8-SO
IMP802LEPA	4.5 to 4.75	–40°C to +85°C	8-Plastic DIP
IMP802LESA	4.5 to 4.75	–40°C to +85°C	8-SO
IMP802M			
IMP802MCPA	4.25 to 4.50	0°C to +70°C	8-Plastic DIP
IMP802MCSA	4.25 to 4.50	0°C to +70°C	8-SO
IMP802MEPA	4.25 to 4.50	–40°C to +85°C	8-Plastic DIP
IMP802MESA	4.25 to 4.50	–40°C to +85°C	8-SO
IMP805L			
IMP805LCPA	4.5 to 4.75	0°C to +70°C	8-Plastic DIP
IMP805LCSA	4.5 to 4.75	0°C to +70°C	8-SO
IMP805LC/D	4.5 to 4.75	25°C	DICE
IMP805LEPA	4.5 to 4.75	–40°C to +85°C	8-Plastic DIP
IMP805LESA	4.5 to 4.75	–40°C to +85°C	8-SO
IMP805LMJA	4.5 to 4.75	Contact Factory	8-CerDIP

Pin Description

Pin Number		Name	Function
IMP690A/IMP692A IMP802L/IMP802M	IMP805L		
1	1	V_{OUT}	Voltage supply for RAM. When V_{CC} is above the reset threshold, V_{OUT} connects to V_{CC} through a P-channel MOS device. If V_{CC} falls below the reset threshold, this output will be connected to the backup supply at V_{BATT} (or V_{CC}, whichever is higher) through the MOS switch to provide continuous power to the CMOS RAM.
2	2	V_{CC}	+5V power supply input
3	3	GND	Ground
4	4	PFI	Power failure monitor input. PFI is connected to the internal power fail comparator which is referenced to 1.25V. The power fail output (PFO) is active LOW but remains HIGH if PFI is above 1.25V. If this feature is unused, the PFI pin should be connected to GND or V_{OUT}.
5	5	$\overline{PFO}$	Power-fail output. $\overline{PFO}$ is active LOW whenever the PFI pin is less than 1.25V.
6	6	WDI	Watchdog input. The WDI input monitors microprocessor activity. An internal timer is reset with each transition of the WDI input. If WDI is held HIGH or LOW for longer than the watchdog timeout period, typically 1.6 seconds, RESET (or $\overline{RESET}$) is asserted for the reset pulse width time, t_{RS}, of 140ms, minimum.
7	——	$\overline{RESET}$	Active-LOW reset output. When triggered by V_{CC} falling below the reset threshold or by watchdog timer timeout, RESET (or $\overline{RESET}$) pulses low for the reset pulse width, t_{RS}, typically 200ms. It will remain low if V_{CC} is below the reset threshold (4.65V in the IMP690A/IMP802L and 4.4V in the IMP692A/IMP802L) and remains low for 200ms after V_{CC} rise above the reset threshold.
——	7	RESET	Active-HIGH reset output. The inverse of $\overline{RESET}$.
8	8	V_{BATT}	Auxiliary power or backup-battery input. V_{BATT} should be connected to GND if the function is not used. This input has about 40mV of hysteresis to prevent rapid toggling between V_{CC} and V_{BATT}.

Absolute Maximum Ratings

Pin Terminal Voltage with Respect to Ground
- V_{CC} . . . . . –0.3V to 6.0V
- V_{BATT} . . . . . –0.3V to 6.0V
- All Other Inputs* . . . . . –0.3V to (V_{CC} + 0.3V)

Input Current at V_{CC} 200mA
Input Current at V_{BATT} 50mA
Input Current at GND 20mA
Output Current:
- V_{OUT} . . . . . Short circuit protected
- All Other Inputs 20mA
- Rate of Rise: V_{BATT} and V_{CC} 100V/µs

Continuous Power Dissipation
- Plastic DIP (derate 9mW/°C above 70°C) . . . 800mW
- SO (derate 5.9mW/°C above 70°C) 500mW
- CerDIP (derate 8mW/°C above 70°C) 650mW

Operating Temperature Range (C Devices) . . . . 0°C to 70°C
Operating Temperature Range (E Devices) . . . . –40°C to 85°C
Storage Temperature Range . . . . . –65°C to 160°C
Lead Temperature Soldering, (10 sec) . . . . . 300°C

** The input voltage limits on PFI and WDI may be exceeded if the current is limited to less than 10mA*

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.

Electrical Characteristics

Unless otherwise noted V_{CC} = 4.75V to 5.5V for the IMP690A/IMP802L/IMP805L and V_{CC} = 4.5V to 5.5V for the IMP692A/IMP802M; V_{BATT} = 2.8V; and $T_A = T_{MIN}$ to T_{MAX}.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
V_{CC}, V_{BATT} Voltage Range (Note 1)		IMP69_AC, IMP802_C		1.1		5.5	V
		IMP805LC		1.1		5.5	
		IMP69_AE, IMP80_ _E		1.1		5.5	
Supply Current Excluding I_{OUT}	I_S	IMP69_AC, IMP802_C			35	100	µA
		IMP69_AE, IMP802_E, IMP805LE			35	100	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, V_{BATT} = 2.8V	T_A = 25°C			1.0	µA
			$T_A = T_{MIN}$ to T_{MAX}			5.0	
V_{BATT} Standby Current (Note 2)		5.5V > V_{CC} > V_{BATT} – 0.2V	T_A = 25°C	–0.1		0.02	µA
			$T_A = T_{MIN}$ to T_{MAX}	–1.0		0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC} – 0.025	V_{CC} – 0.010		V
		I_{OUT} = 50mA		V_{CC} – 0.25	V_{CC} – 0.10		
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT} – 0.2V		V_{BATT} – 0.1	V_{BATT} – 0.001		V
Battery Switch Threshold, V_{CC} to V_{BATT}		V_{CC} < V_{RT}	Power-up		20		mV
			Power-down		–20		
Battery Switchover Hysteresis					40		mV
Reset Threshold	V_{RT}	IMP690A/802L/805L		4.50	4.65	4.75	V
		IMP692A, IMP802M		4.25	4.40	4.50	
		IMP802L, T_A = 25°C, V_{CC} falling		4.55		4.70	
		IMP802M, T_A = 25°C, V_{CC} falling		4.30		4.45	
Reset Threshold Hysteresis					40		mV
Reset Pulse Width	t_{RS}			140	200	280	ms
Reset Output Voltage		I_{SOURCE} = 800µA		V_{CC} – 1.5			V
		I_{SINK} = 3.2mA				0.4	
		IMP69_AC, IMP802_C, V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		IMP69_AE, IMP802_E, V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	
		IMP805LC, I_{SOURCE} = 4µA, V_{CC} = 1.1V		0.8			
		IMP805LE, I_{SOURCE} = 4µA, V_{CC} = 1.2V		0.9			
		IMP805L, I_{SOURCE} = 800µA		V_{CC} – 1.5			
		IMP805L, I_{SINK} = 3.2mA				0.4	
Watchdog Timeout	t_{WD}			1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}		50			ns
WDI Input Current		WDI = V_{CC}			50	150	µA
		WDI = 0V		–150	–50		
WDI Input Threshold (Note 3)		V_{CC} = 5V, Logic LOW				0.8	V
		V_{CC} = 5V, Logic HIGH		3.5			
PFI Input Threshold		IMP69_A, IMP805L, V_{CC} = 5V		1.20	1.25	1.30	V
		IMP802_C/E, V_{CC} = 5V		1.225	1.250	1.275	
PFI Input Current				–25	0.01	25	nA
PFO Output Voltage		I_{SOURCE} = 800µA		V_{CC} – 1.5			V
		I_{SINK} = 3.2mA				0.4	

Notes: 1. If V_{CC} or V_{BATT} is 0V, the other must be greater than 2.0V.
2. Battery charging-current is "–". Battery discharge-current is "+".
3. WDI is guaranteed to be in an intermediate level state if WDI is floating and V_{CC} is within the operating voltage range. WDI input impedance is 50kΩ. WDI is biased to 0.3V_{CC}.

Application Information

Reset Output

It is important to initialize a microprocessor to a known state in response to specific events that could create code execution errors and "lock-up". The reset output of these supervisory circuits send a reset pulse to the microprocessor in response to power-up, power-down/power-loss or a watchdog time-out. The reset pulse width, t_{RS}, is typically around 200ms and is LOW for the IMP690A, IMP692A, IMP802 and HIGH for the IMP805L.

Power-up reset occurs when a rising V_{CC} reaches the reset threshold, V_{RT}, forcing a reset condition in which the reset output is asserted in the appropriate logic state for the duration of t_{RS}. *Figure 2* shows the reset pin timing.

Power-loss or "brown-out" reset occurs when V_{CC} dips below the reset threshold resulting in a reset assertion for the duration of t_{RS}.

The reset signal remains asserted as long as V_{CC} is between V_{RT} and 1.1V, the lowest V_{CC} for which these devices can provide a guaranteed logic-low output. To ensure logic inputs connected to the IMP690A/692A/802 RESET pin are in a known state when V_{CC} is under 1.1V, a 100kΩ pull-down resistor at RESET is needed: the logic-high IMP805L will need a pull-up resistor to V_{CC}.

A Watchdog time-out reset occurs when a logic "1" or logic "0" is continuously applied to the WDI pin for more than 1.6 seconds. After the duration of the reset interval, the watchdog timer starts a new 1.6 second timing interval; the microprocessor must service the watchdog input by changing states or by floating the WDI pin before this interval is finished. If the WDI pin is held either HIGH or LOW, a reset pulse will be triggered every 1.8 seconds (the 1.6 second timing interval plus the reset pulse width t_{RS}).

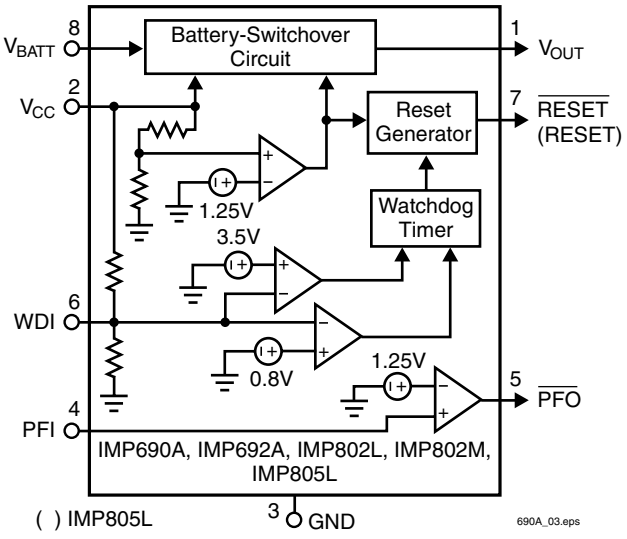


Figure 1. Block Diagram

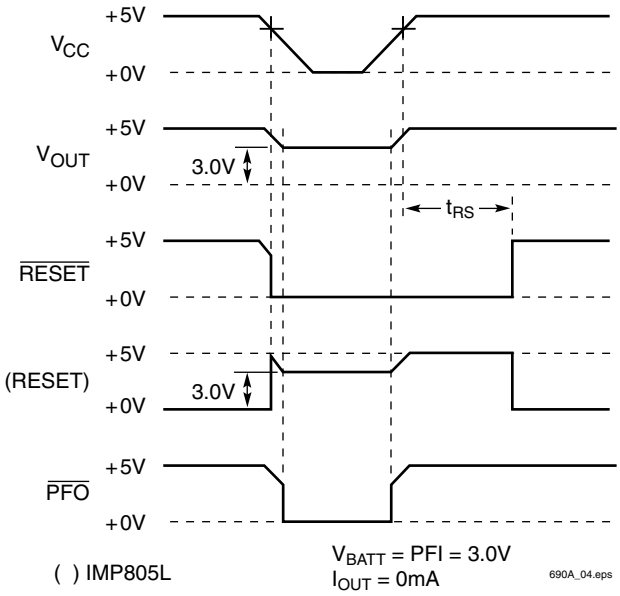


Figure 2. Timing Diagram

Application Information

Microprocessor Interface.

The IMP690 has logic-LOW RESET output while the IMP805 has an inverted logic-HIGH RESET output. Microprocessors with bi-directional reset pins (69HC11 for example) can pose a problem when the supervisory circuit and the microprocessor output pins attempt to go to opposite logic states. The problem can be resolved by placing a 4.7kΩ resistor between the RESET output and the microprocessor reset pin. This is shown in *Figure 3*. Since the series resistor limits drive capabilities, the reset signal to other devices should be buffered.

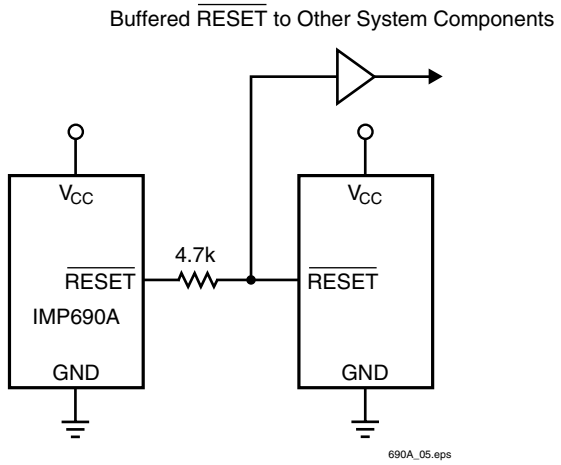


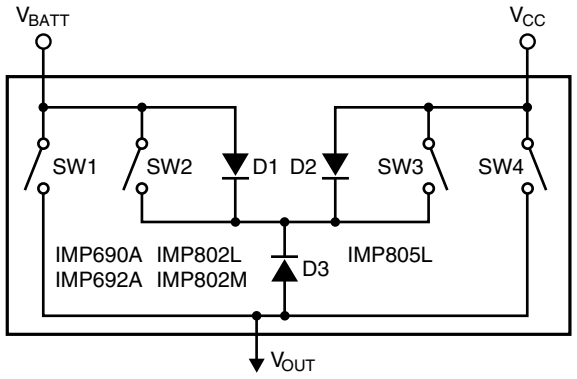
Figure 3. Interfacing with bi-directional microprocessor reset inputs

Watchdog Input

As discussed in the Reset section, the Watchdog Input is used to monitor microprocessor activity. It can be used to insure that the microprocessor is in a continually responsive state by requiring that the WDI pin be toggled every second. If the WDI pin is not toggled within the 1.6 second window (minimum t_{WD} + t_{RS}), a reset pulse will be asserted to return the microprocessor to the initial start-up state. Pulses as short as 50ns can be applied to the WDI pin. If this feature is not used, the WDI pin should be open-circuited or the logic placed into a high-impedance state to allow the pin to float.

Backup-Battery Switchover

A power loss can be made less severe if the system RAM contents are preserved. This is achieved in the IMP690/692/802/805 by switching from the failed V_{CC} to an alternate power source connected at V_{BATT} when V_{CC} is less than the reset threshold voltage (V_{CC} < V_{RT}), and V_{CC} is less than V_{BATT}. The V_{OUT} pin is normally connected to V_{CC} through a 2Ω PMOS switch but a brown-out or loss of V_{CC} will cause a switchover to V_{BATT} by means of a 20Ω PMOS switch. Although both conditions (V_{CC} < V_{RT} and V_{CC} < V_{BATT}) must occur for the switchover to V_{BATT} to occur, V_{OUT} will be switched back to V_{CC} when V_{CC} exceeds V_{RT} irrespective of the voltage at V_{BATT}. It should be noted that an internal device diode (D1 in *Figure 4*) will be forward biased if V_{BATT} exceeds V_{CC} by more than a diode drop when V_{CC} is switched to V_{OUT}. Because of this it is recommended that V_{BATT} be no greater than V_{RT} +0.6V.



CONDITION	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and V_{CC} > V_{BATT}	Open	Closed
V_{CC} < Reset Threshold and V_{CC} < V_{BATT}	Closed	Open

IMP690A/IMP802L/IMP805L Reset Threshold = 4.65V
IMP692A/IMP802M Reset Threshold = 4.4V

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Figure 4. Internal device configuration of battery switch-over function

Application Information

Table 1. Pin Connections in Battery Backup Mode

Pin	Connection
V_{OUT}	Connected to V_{BATT} through internal PMOS switch
V_{BATT}	Connected to V_{OUT}
PFI	Disabled
$\overline{PFO}$	Logic-LOW
$\overline{RESET}$	Logic LOW (except on IMP805 where it is HIGH)
WDI	Watchdog timer disabled

During the backup power mode, the internal circuitry of the supervisory circuit draws power from the battery supply. While V_{CC} is still alive, the comparator circuits remain alive and the current drawn by the device is typically 35µA. When V_{CC} drops more than 1.1V below V_{BATT}, the internal switchover comparator, the PFI comparator and WDI comparator will shut off, reducing the quiescent current drawn by the IC to less than 1µA.

Backup Power Sources - Batteries

Battery voltage selection is important to insure that the battery does not discharge through the parasitic device diode D1 (see *Figure 4*) when V_{CC} is less than V_{BATT} and $V_{CC} > V_{RT}$.

Table 2. Maximum Battery Voltages

Part No.	MAXIMUM Battery Voltage
IMP690A	4.80
IMP802L	4.80
IMP805L	4.80
IMP692A	4.55
IMP802M	4.55

Although most batteries that meet the requirements of *Table 2* are acceptable, lithium batteries are very effective backup source due to their high-energy density and very low self-discharge rates.

Battery Replacement while Powered

Batteries can be replaced even when the device is in a powered state as long as V_{CC} remains above the reset threshold voltage V_{RT}. In the IMP devices, a floating V_{BATT} pin will not cause a power-supply switchover as can occur in some other supervisory circuits. If V_{BATT} is not used, the pin should be grounded.

Backup Power Sources - SuperCap™

Capacitor storage, with very high values of capacitance, can be used as a back-up power source instead of batteries. SuperCap™ are capacitors with capacities in the fractional farad range. A 0.1 farad SuperCap™ would provide a useful backup power source. Like the battery supply, it is important that the capacitor voltage remain below the maximum voltages shown in *Table 2*. Although the circuit of *Figure 5* shows the most simple way to connect the SuperCap™, this circuit cannot insure that an overvoltage condition will not occur since the capacitor will ultimately charge up to V_{CC}. To insure that an overvoltage condition does not occur, the circuit of *Figure 6* is preferred. In this circuit configuration, the diode-resistor pair clamps the capacitor voltage at one diode-drop below V_{CC}. V_{CC} itself should be regulated within ±5% of 5V for the IMP692A/802M or within ±10% of 5V for the IMP690A/802L/805L to insure that the storage capacitor does not achieve an overvoltage state.

Note: SuperCap™ is a trademark of Baknor Industries

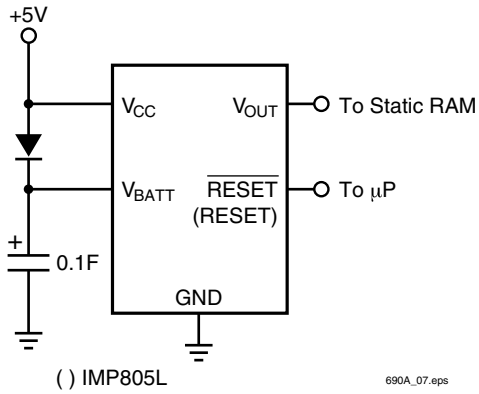


Figure 5. Capacitor as a backup power source

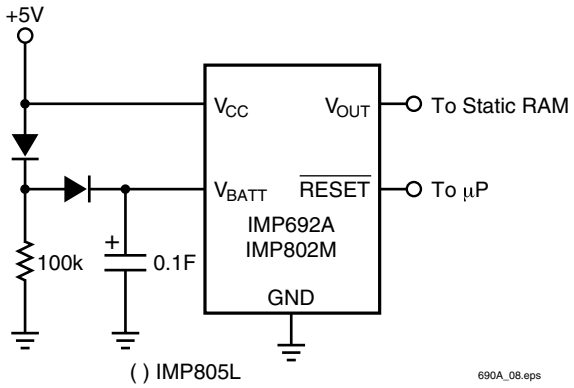


Figure 6. Capacitor as back-up Power Source - Voltage clamped to 0.5V below V_{CC}

Application Information

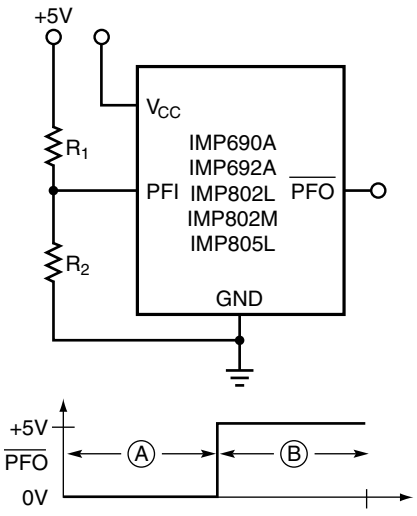
Operation Without a Backup Power Source

When operating without a back-up power source, the V_{BATT} pin should be connected to GND and V_{OUT} should be connected to V_{CC}, since power source switchover will not occur. Connecting V_{OUT} to V_{CC} eliminates the voltage drop due to the ON-resistance of the PMOS switch.

Power-Fail Comparator

The Power Fail feature is an independent voltage monitoring function that can be used for any number of monitoring activities. The PFI function can provide an early sensing of power supply failure by sensing the voltage of the unregulated DC ahead of the regulated supply sensing seen by the backup-battery switchover circuitry.

The PFI pin is compared to a 1.25V internal reference. If the voltage at the PFI pin is less than this reference voltage, the $\overline{PFO}$ pin goes low. By sensing the voltage of the raw DC power supply, the microprocessor system can prepare for imminent power-loss, especially if the battery backup supply is not enabled. The input voltage at the PFI pin results from a simple resistor voltage divider as shown in *Figure 7*.

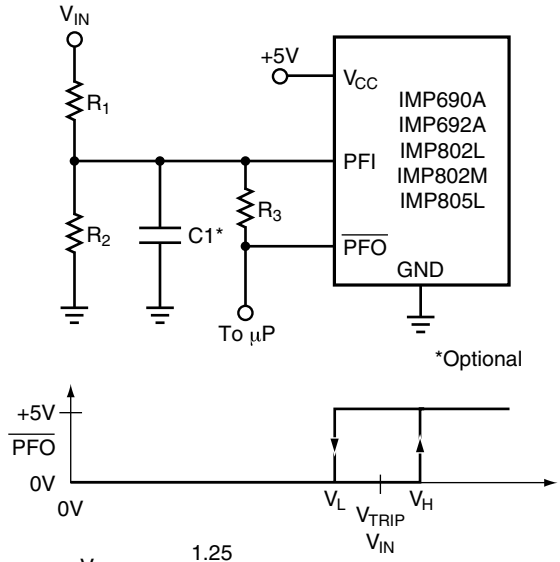


Ⓐ $\frac{5R_2}{R_1+R_2} < 1.25V$ Ⓑ $\frac{5R_2}{R_1+R_2} > 1.25V$

Figure 7. Simple Voltage divider sets PFI trip point

Power Fail Hysteresis

A noise margin can be added to the simple monitoring circuit of *Figure 7* by adding positive feedback from the $\overline{PFO}$ pin. The circuit of *Figure 8* adds this positive "latching" effect by means of an additional resistor R3 connected between $\overline{PFO}$ and PFI which helps in pulling PFI in the direction of $\overline{PFO}$ and eliminating an indecision at the trip point. Resistor R3 is normally about 10 times higher in resistance than R2 to keep the hysteresis band reasonable and should be larger than 10kΩ to avoid excessive loading on the $\overline{PFO}$ pin. The calculations for the correct values of resistors to set the hysteresis thresholds are given in *Figure 8*. A capacitor can be added to offer additional noise rejection by low-pass filtering.



$$V_{TRIP} = \frac{1.25}{\left(\frac{R_2}{R_2+R_2}\right)}$$

$$V_{IH} = \frac{1.25}{\left(\frac{R_2 \| R_3}{R_1+R_2 \| R_3}\right)}$$

$$\frac{V_L - 1.25}{R_1} + \frac{5-1.25}{R_3} = \frac{1.25}{R_2}$$

Figure 8. Hysteresis added to PFI pin

Monitoring Capabilities of the Power-Fail Input

Although designed for power supply failure monitoring, the PFI pin can be used for monitoring any voltage condition that can be scaled by means of a resistive divider. An example is the negative power supply monitor configured in *Figure 9*. In this case a good negative supply will hold the PFI pin below 1.25V and the $\overline{PFO}$ pin will be at a logic "0". As the negative voltage declines, the voltage at the PFI pin will rise until it exceeds 1.25V and the $\overline{PFO}$ pin will go to a logic "1".

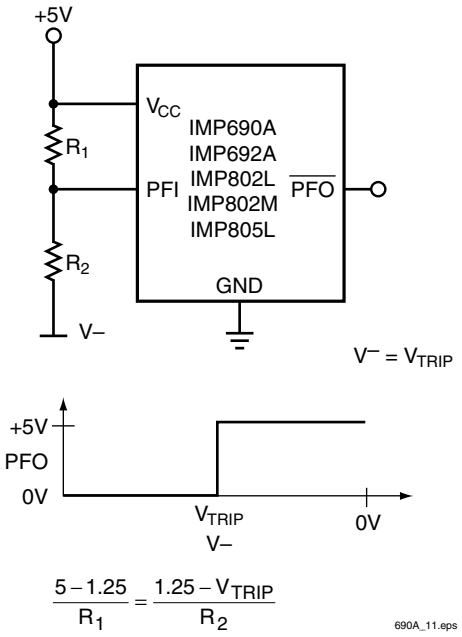
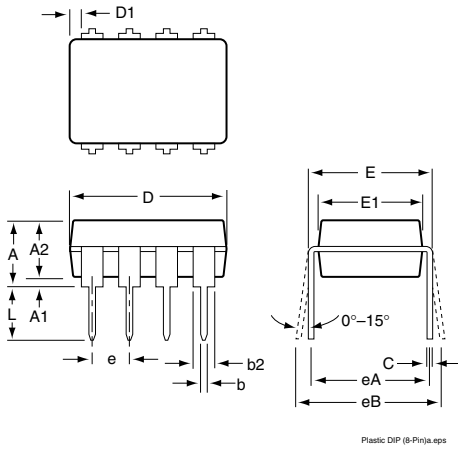


Figure 9. Using PFI to monitor negative supply voltage

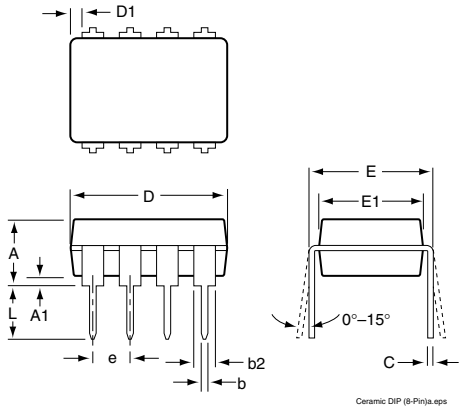
Package Dimensions

Plastic DIP (8-Pin)



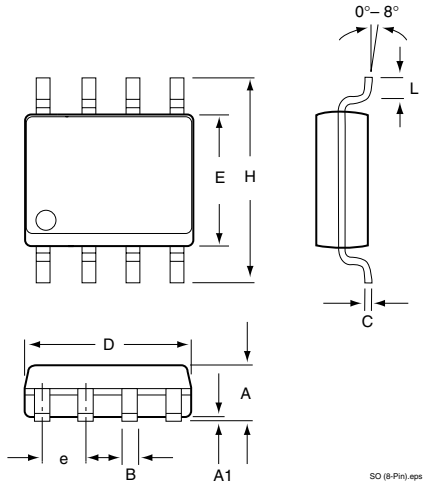
Plastic DIP (8-Pin)a.eps

CerDIP (8-Pin)



Ceramic DIP (8-Pin)a.eps

SO (8-Pin)



SO (8-Pin).eps

	Inches		Millimeters	
	Min	Max	Min	Max
Plastic DIP (8-Pin)*				
A	———	0.210	———	5.33
A1	0.015	———	0.38	———
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
b3	0.030	0.045	0.80	1.14
D	0.355	0.400	9.02	10.16
D1	0.005	———	0.13	———
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	———	2.54	
eA	0.300	———	7.62	
eB	———	0.430	———	10.92
eC	———	0.060		
L	0.115	0.150	2.92	3.81
CerDIP (8-Pin)				
A	———	0.200	———	5.08
A1	0.015	0.070	0.38	1.78
b	0.014	0.023	0.36	0.58
b2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	———	0.405	———	10.29
D1	0.005	———	0.13	———
E	0.290	0.320	7.37	8.13
E1	0.220	0.310	5.59	7.87
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
SO (8-Pin)**				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
D	0.189	0.197	4.80	5.00

** JEDEC Drawing MS-001BA*
*** JEDEC Drawing MS-012AA*

Low-Power µP Supervisor Circuits

- Watchdog timer
- Brownout detection
- Power supply monitor

The IMP705/706/707/708 and IMP813L CMOS supervisor circuits monitor power-supply and battery voltage level, and µP/µC operation. Compared to pin-compatible devices offered by Maxim Integrated Products, IMP devices feature 60 percent lower maximum supply current.

The family offers several functional options. Each device generates a reset signal during power-up, power-down and during brownout conditions. A reset is generated when the supply drops below 4.65V (IMP705/707/813L) or 4.40V (IMP706/708). For 3V power supply applications, refer to the IMP705P/R/S/T data sheet. In addition, the IMP705/706/813L feature a 1.6 second watchdog timer. The IMP707/708 have both active-HIGH and active-LOW reset outputs but no watchdog function. The IMP813L has the same pin-out and functions as the IMP705 but has an active-HIGH reset output. A versatile power-fail circuit has a 1.25V threshold, useful in checking battery levels and non-5V supplies. All devices have a manual reset ($\overline{MR}$) input. The watchdog timer output will trigger a reset if connected to $\overline{MR}$.

All devices are available in 8-pin DIP, SO and MicroSO packages.

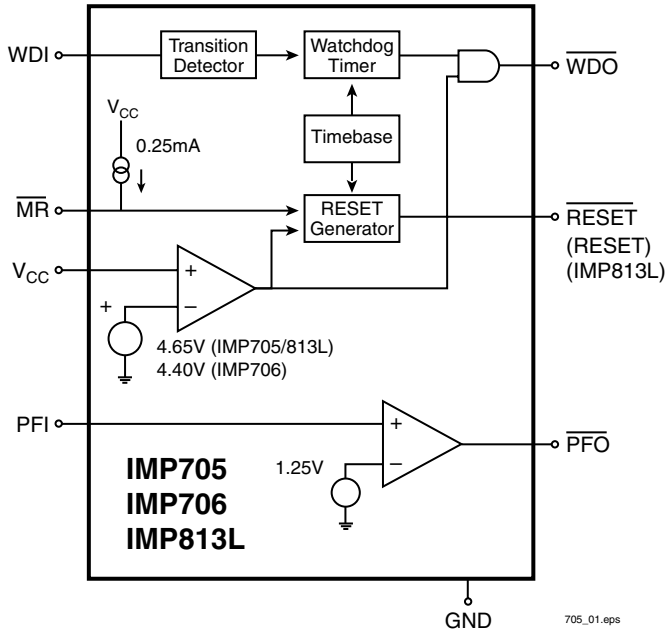
Key Features

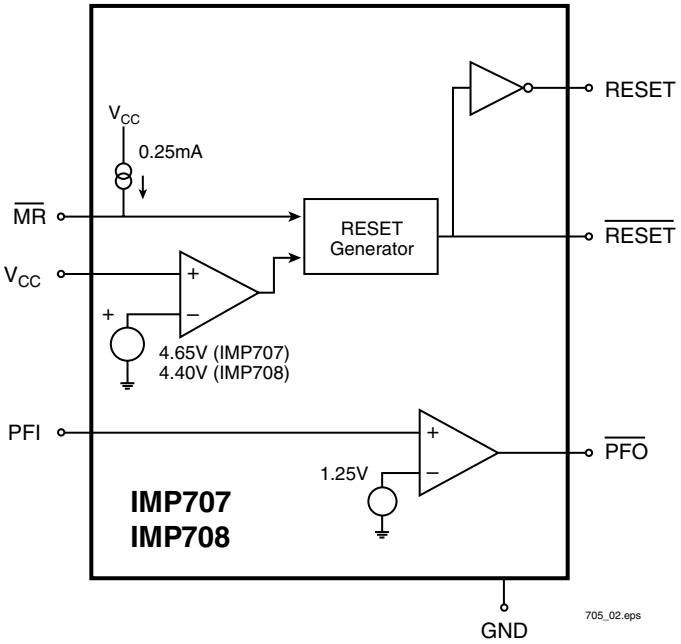
- Improved replacements for the Maxim MAX705/6/7/8, MAX813L
  - 140µA maximum supply current
  - 60% improvement
- Precision power supply monitor
  - 4.65V threshold (IMP705/707/813L)
  - 4.40V threshold (IMP706/8)
- Debounced manual reset input
- Voltage monitor
  - 1.25V threshold
  - Battery monitor/Auxiliary supply monitor
- Watchdog timer (IMP705/706/813L)
- 200ms reset pulse width
- Active HIGH reset output (IMP707/708/813L)
- MicroSO package

Applications

- Computers and embedded controllers
- Battery-operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment

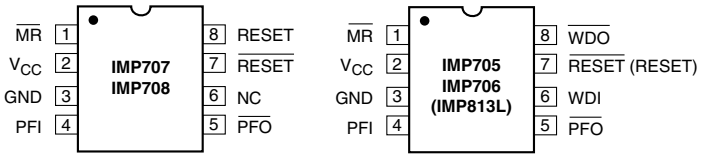
Block Diagrams



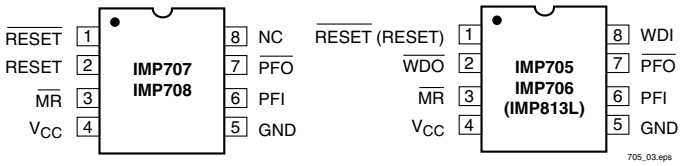


Pin Configuration

DIP/SO



MicroSO



Ordering Information

Part Number	Reset Threshold (V)	Temperature Range	Pins-Package
IMP705 Active LOW Reset, Watchdog Output and Manual RESET			
IMP705CPA	4.65	0°C to +70°C	8-Plastic DIP
IMP705CSA	4.65	0°C to +70°C	8-SO
IMP705CUA	4.65	0°C to +70°C	8-MicroSO
IMP705C/D	4.65	25°C	Dice
IMP705EPA	4.65	–40°C to +85°C	8-Plastic DIP
IMP705ESA	4.65	–40°C to +85°C	8-SO
IMP706ESA	4.40	–40°C to +85°C	8-SO
IMP706 Active LOW Reset, Watchdog Output and Manual RESET			
IMP706CPA	4.40	0°C to +70°C	8-Plastic DIP
IMP706CSA	4.40	0°C to +70°C	8-SO
IMP706CUA	4.40	0°C to +70°C	8-MicroSO
IMP706C/D	4.40	25°C	Dice
IMP706EPA	4.40	–40°C to +85°C	8-Plastic DIP
IMP706ESA	4.40	–40°C to +85°C	8-SO
IMP707 Active LOW & HIGH Reset with Manual RESET			
IMP707CPA	4.65	0°C to +70°C	8-Plastic DIP
IMP707CSA	4.65	0°C to +70°C	8-SO
IMP707CUA	4.65	0°C to +70°C	8-MicroSO
IMP707C/D	4.65	25°C	Dice
IMP707EPA	4.65	–40°C to +85°C	8-Plastic DIP
IMP707ESA	4.65	–40°C to +85°C	8-SO
IMP708 Active LOW & HIGH Reset with Manual RESET			
IMP708CPA	4.40	0°C to +70°C	8-Plastic DIP
IMP708CSA	4.40	0°C to +70°C	8-SO
IMP708CUA	4.40	0°C to +70°C	8-MicroSO
IMP708C/D	4.40	25°C	Dice
IMP708EPA	4.40	–40°C to +85°C	8-Plastic DIP
IMP708ESA	4.40	–40°C to +85°C	8-SO
IMP813L Active HIGH Reset, Watchdog Output and Manual RESET			
IMP813LCPA	4.65	0°C to +70°C	8-Plastic DIP
IMP813LCSA	4.65	0°C to +70°C	8-SO
IMP813LCUA	4.65	0°C to +70°C	8-MicroSO
IMP813LC/D	4.65	25°C	Dice
IMP813LEPA	4.65	–40°C to +85°C	8-Plastic DIP
IMP813LESA	4.65	–40°C to +85°C	8-SO

Absolute Maximum Ratings

Pin Terminal Voltage with Respect to Ground

V_{CC} . . . . . –0.3V to 6.0V
All other inputs[1] . . . . . –0.3V to (V_{CC} + 0.3V)
Input Current at V_{CC} and GND 20mA
Output Current: All outputs 20mA
Rate of Rise at V_{CC} 100V/µs
Plastic DIP Power Dissipation . . . . . 700 mW
(Derate 9 mW/°C above 70°C)
SO Power Dissipation . . . . . 470 mW
(Derate 5.9 mW/°C above 70°C)
MicroSO Power Dissipation 330mW
(Derate 4.1 mW/°C above 70°C)

Operating Temperature Range

IMP705E/706E/707E/708E/813LE . . . . . –40°C to 85°C
IMP706C/707C/708C/813LC . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to 160°C
Lead Temperature Soldering(10 sec) . . . . . 300°C

Note: 1. The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

These are stress ratings only and functional operation is not implied.

Electrical Characteristics

Unless otherwise noted, V_{CC} = 4.75V to 5.5V for the IMP705/707/813L. V_{CC} = 4.5V to 5.5V for the IMP706/708 and over the operating temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage Range	V_{CC}	IMP705/6/7/8C	1.2		5.5	V
		IMP813L	1.1		5.5	
		IMP705/6/7/8E, IMP813lE	1.2		5.5	
Supply Current	I_{CC}	IMP705C/706C/813LC		75	140	µA
		IMP705E, IMP706E, IMP813LE		75	140	
		IMP707C, IMP708C		50	140	
		IMP707E, IMP708E		50	140	
RESET Threshold	V_{RT}	IMP705, IMP707, IMP813L, Note 2	4.50	4.65	4.75	V
		IMP706, IMP708, Note 2	4.25	4.40	4.50	
RESET Threshold Hysteresis		Note 2		40		mV
RESET Pulse Width	t_{RS}	Note 2	140	200	280	ms
$\overline{MR}$ Pulse Width	t_{MR}		0.15			µs
$\overline{MR}$ to RESET Out Delay	t_{MD}	Note 2			0.25	µs
$\overline{MR}$ Input Threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
$\overline{MR}$ Pull-up Current		$\overline{MR}$ = 0V	100	250	600	µA
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5V			V
		I_{SINK} = 3.2mA			0.4	
		IMP705/6/7/8, V_{CC} = 1.2V, I_{SINK} = 100µA			0.3	
RESET Output Voltage		IMP707/708/813L, I_{SOURCE} = 800µA	V_{CC} - 1.5V			V
		IMP707/708, I_{SINK} = 1.2mA			0.4	
		IMP813L, I_{SINK} = 3.2mA			0.4	
		IMP813L, V_{CC} =1.2V, I_{SOURCE} = 4µA	0.9			
Watchdog Timeout Period	t_{WD}	IMP705/706/813L	1.00	1.60	2.25	s
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}	50			ns
WDI Input Threshold	V_{IH}	IMP705/706/813L, V_{CC} = 5V	3.5			V
	V_{IL}				0.8	
WDI Input Current		IMP705/706/813L, WDI = V_{CC}		50	150	µA
		IMP705/706/813L, WDI = 0V	–150	–50		
$\overline{WDO}$ Output Voltage		IMP705/706/813L, I_{SOURCE} = 800µA	V_{CC} - 1.5V			V
		IMP705/706/813L, I_{SINK} = 1.2mA			0.4	
PFI Input Threshold		V_{CC} = 5V	1.2	1.25	1.3	V
PFI Input Current			–25	0.01	25	nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5V			V
		I_{SINK} = 3.2mA			0.4	

Notes: 2. $\overline{RESET}$ (IMP705/6/7/8), RESET (IMP707/8, IMP813L)

Pin Descriptions

Pin Number						Name	Function
IMP705/706		IMP707/708		IMP813L			
DIP/SO	MicroSO	DIP/SO	MicroSO	DIP/SO	MicroSO		
1	3	1	3	1	3	$\overline{MR}$	Manual RESET input. The active LOW input triggers a reset pulse. A 250µA pull-up current allows the pin to be driven by TTL / CMOS logic or shorted to ground with a switch.
2	4	2	4	2	4	V_{CC}	+5V power supply input.
3	5	3	5	3	5	GND	Ground reference for all signals.
4	6	4	6	4	6	PFI	Power-fail voltage monitor input. With PFI less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to ground or V_{CC} when not used.
5	7	5	7	5	7	$\overline{PFO}$	Power-fail output. The output is active LOW and sinks current when PFI is less than 1.25V.
6	8	—	—	6	8	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 1.6sec at WDI allows the internal timer to run-out, setting $\overline{WDO}$ LOW. The watchdog function is disabled by floating WDI or by connecting WDI to a high-impedance three-state buffer. The internal watchdog timer clears when: RESET is asserted; WDI is three-stated; or WDI sees a rising or falling edge.
—	—	6	—	—	—	NC	Not connected.
7	1	7	1	—	—	$\overline{RESET}$	Active-LOW reset output. Pulses LOW for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold (IMP705: 4.65V, IMP705J: 4.00V, IMP706: 4.40V). $\overline{RESET}$ remains LOW for 200ms after V_{CC} rises above the RESET threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	2	—	—	8	2	$\overline{WDO}$	Watchdog output. $\overline{WDO}$ pulls LOW when the 1.6 sec internal watchdog timer times-out and does not go HIGH until the watchdog is cleared. In addition, when V_{CC} is below the reset threshold, $\overline{WDO}$ remains low. Unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width and as soon as V_{CC} exceeds the reset threshold, $\overline{WDO}$ goes HIGH with no delay.
—	—	8	2	7	1	RESET	Active-HIGH reset output. RESET is the inverse of $\overline{RESET}$. The IMP813L has only a RESET output.

Feature Summary

	IMP705	IMP706	IMP707	IMP708	IMP813L
Power-fail detector	■	■	■	■	■
Brownout detection	■	■	■	■	■
Manual RESET input	■	■	■	■	■
Power-up/down RESET	■	■	■	■	■
Watchdog timer	■	■			■
Active-HIGH RESET output			■	■	■
Active-LOW RESET output	■	■	■	■	
RESET threshold	4.65V/4.00V	4.40V	4.65V	4.40V	4.65V

Detail Descriptions

RESET/$\overline{\text{RESET}}$ Operation

The RESET/$\overline{\text{RESET}}$ signals are designed to start a µP/µC in a known state or return the system to a known state.

The IMP707/708 have two RESET outputs, one active-HIGH RESET and one active-LOW RESET output. The IMP813L has only an active-HIGH output. RESET is simply the complement of $\overline{\text{RESET}}$.

$\overline{\text{RESET}}$ is guaranteed to be LOW with V_{CC} above 1.2V. During a power-up sequence, $\overline{\text{RESET}}$ remains low until the supply rises above the threshold level, either 4.65V, 4.40V or 4.00V. $\overline{\text{RESET}}$ goes high approximately 200ms after crossing the threshold.

During power-down, $\overline{\text{RESET}}$ goes LOW as V_{CC} falls below the threshold level and is guaranteed to be under 0.4V with V_{CC} above 1.2V.

In a brownout situation where V_{CC} falls below the threshold level, $\overline{\text{RESET}}$ pulses low. If a brownout occurs during an already-initiated reset, the pulse will continue for a minimum of 140ms.

Auxiliary Comparator

All devices have an auxiliary comparator with 1.25V trip point and uncommitted output ($\overline{\text{PFO}}$) and noninverting input (PFI). This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the $\overline{\text{PFO}}$ output to transit LOW. Normally $\overline{\text{PFO}}$ interrupts the processor so the system can be shut down in a controlled manner.

Manual Reset ($\overline{\text{MR}}$)

The active-LOW manual reset input is pulled high by a 250µA pull-up current and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140ms minimum reset time will debounce mechanical pushbutton switches.

By connecting the watchdog output ($\overline{\text{WDO}}$) and $\overline{\text{MR}}$, a watchdog timeout forces $\overline{\text{RESET}}$ to be generated. The IMP813L should be used when an active-HIGH RESET is required.

Watchdog Timer

The watchdog timer available on the IMP705/706/813L monitors µP/µC activity. If activity is not detected within 1.6 seconds, the internal timer puts the watchdog output, $\overline{\text{WDO}}$, into a LOW state. $\overline{\text{WDO}}$ will remain LOW until activity is detected at WDI.

The watchdog function is disabled, meaning it is cleared and not counting, if WDI is floated or connected to a three-stated circuit. The watchdog timer is also disabled if RESET is asserted. When RESET becomes inactive and the WDI input sees a high or low transition as short as 50ns, the watchdog timer will begin a 1.6 second countdown. Additional transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

$\overline{\text{WDO}}$ will also become LOW and remain so, whenever the supply voltage, V_{CC} , falls below the device threshold level. $\overline{\text{WDO}}$ goes HIGH as soon as V_{CC} transitions above the threshold. There is no minimum pulse width for $\overline{\text{WDO}}$ as there is for the RESET outputs. If WDI is floated, $\overline{\text{WDO}}$ essentially acts as a low-power output indicator.

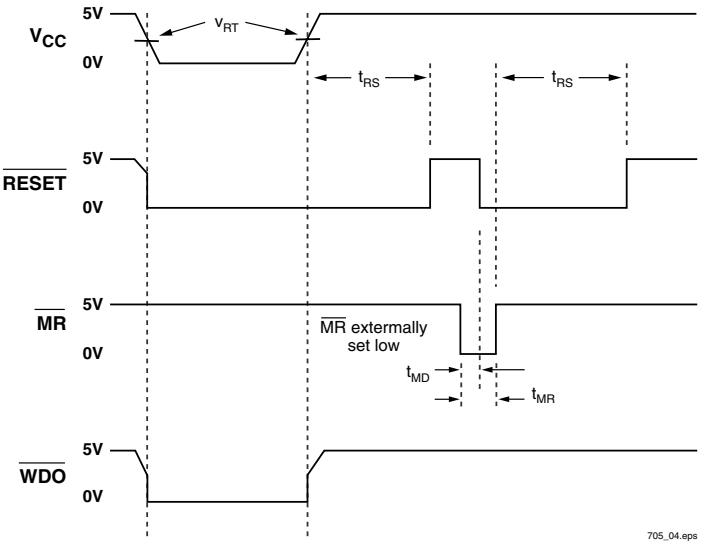


Figure 1. WDI Three-state operation

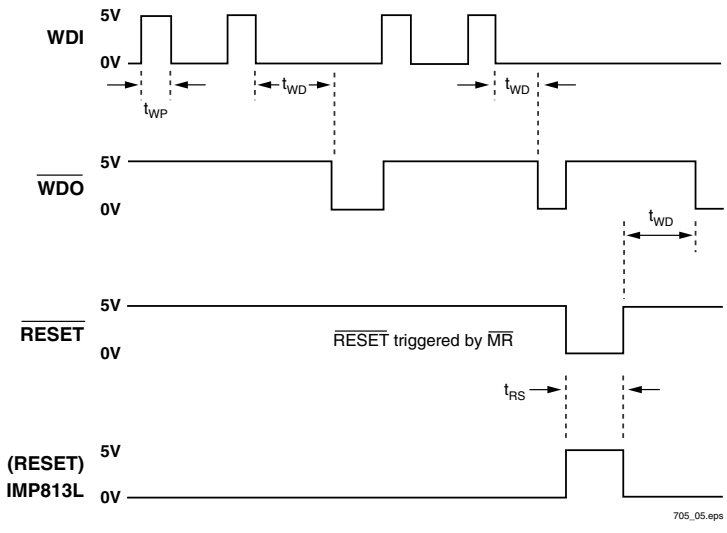


Figure 2. Watchdog Timing

Application Information

Ensuring That RESET is Valid Down to V_{CC} = 0V

When V_{CC} falls below 1.1V, the IMP705-708 RESET output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force RESET to the wrong state, a pull-down resistor should be connected to the RESET pin, thus draining such charges to ground and holding RESET low. The resistor value is not critical. A 100kΩ resistor will pull RESET to ground without loading it.

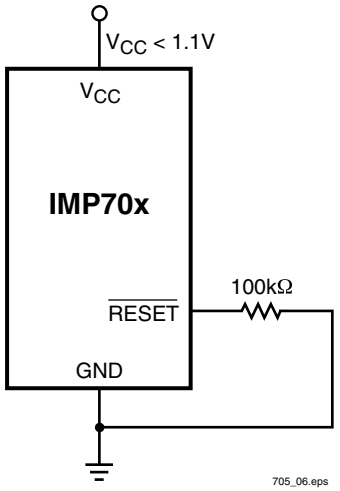


Figure 3. Ensuring That RESET is Valid Down to V_{CC} = 0V

Bi-directional Reset Pin Interfacing

The IMP705/6/7/8 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the RESET output and the µP/µC bi-directional RESET pin.

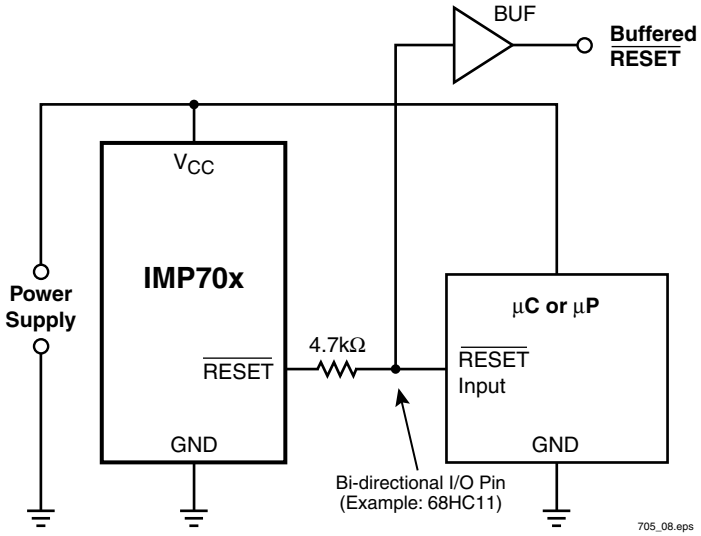


Figure 3. Bi-directional Reset Pin Interfacing

Application Information

Monitoring Voltages Other Than V_{CC}

The IMP705-708 can monitor voltages other than V_{CC} using the Power Fail circuitry. If a resistive divider is connected from the voltage to be monitored to the Power Fail input, PFI, the PFO (output) will go LOW if the divider voltage goes below its 1.25V reference. Should hysteresis be desired, connect a resistor (equal to approximately 10 times the sum of the two resistors in the divider) between the PFI and PFO pins. A capacitor between PFI and GND will reduce circuit sensitivity to input high-frequency noise. If it is desired to assert a RESET in addition to the PFO flag, this may be achieved by connecting the PFO output to MR.

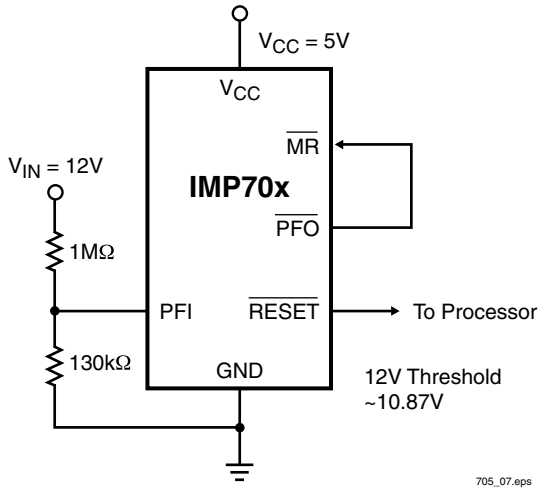


Figure 4. Monitoring Voltages Other Than V_{CC}

Monitoring a Negative Voltage

The Power-Fail circuitry can also monitor a negative supply rail. When the negative rail is OK, PFO will be LOW, and when the negative rail is failing (not negative enough), PFO goes HIGH (the opposite of when positive voltages are monitored). To trigger a reset, these outputs need to be inverted: adding the resistors and transistor as shown achieves this. The RESET output will then have the same sense as for positive voltages: good = HIGH, bad = LOW. It should be noted that this circuit's accuracy depends on the V_{CC} line, the PFI threshold tolerance, and the resistors.

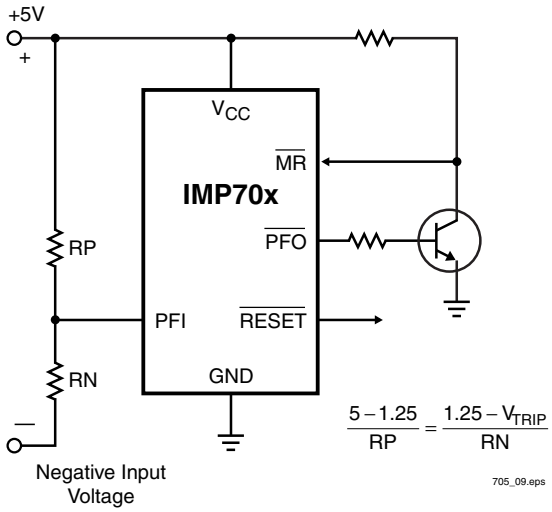
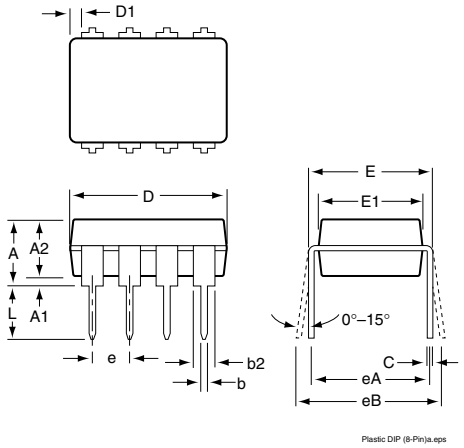


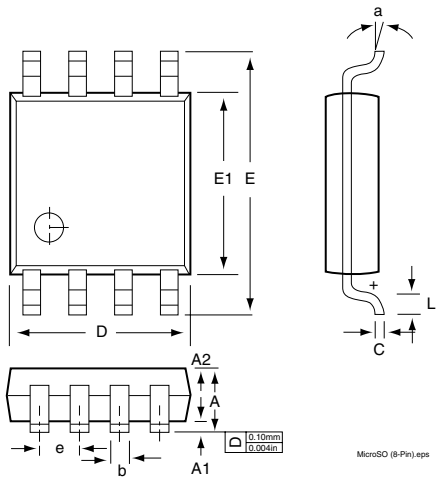
Figure 5. Monitoring a Negative Voltage

Package Dimensions

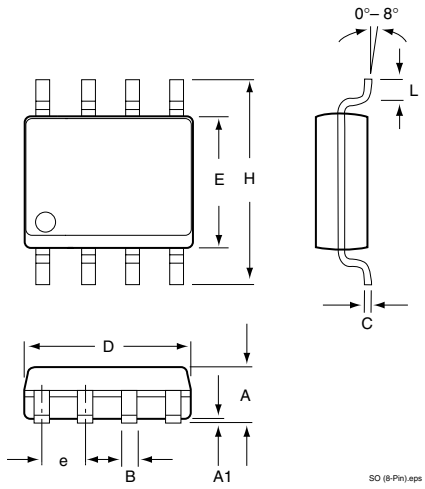
Plastic DIP (8-Pin)*



MicroSO (8-Pin)**



SO (8-Pin)***



	Inches		Millimeters	
	Min	Max	Min	Max
Plastic DIP (8-Pin)				
A	———	0.210	———	5.33
A1	0.015	———	0.38	———
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
b3	0.030	0.045	0.80	1.14
D	0.355	0.400	9.02	10.16
D1	0.005	———	0.13	———
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	———	2.54	
eA	0.300	———	7.62	
eB	———	0.430	———	10.92
eC	———	0.060		
L	0.115	0.150	2.92	3.81
MicroSO (8-Pin)				
A	———	0.0433	———	1.10
A1	0.0020	0.0059	0.050	0.15
A2	0.0295	0.0374	0.75	0.95
b	0.0098	0.0157	0.25	0.40
C	0.0051	0.0091	0.13	0.23
D	0.1142	0.1220	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.193 BSC		4.90 BSC	
E1	0.1142	0.1220	2.90	3.10
L	0.0157	0.0276	0.40	0.70
a	0°	6°	0°	6°
SO (8-Pin)				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
D	0.189	0.197	4.80	5.00

** JEDEC Drawing MS-001BA*
*** JEDEC Drawing MO-187AA*
**** JEDEC Drawing MS-012AA*

3-Pin Microcontroller Power Supply Supervisor

The IMP809/IMP810 are 3.0V, 3.3V and 5.0V power supply supervisor circuits optimized for low-power microprocessor (µP), microcontroller (µC) and digital systems. The IMP809/810 are improved drop-in replacements for the Maxim MAX809/810 and feature 60% lower supply current.

A reset signal is issued if the power supply voltage drops below a preset reset threshold and is asserted for at least 140ms after the supply has risen above the reset threshold. The IMP809 has an active-low $\overline{\text{RESET}}$ output that is guaranteed to be in the correct state for V_{CC} down to 1.1V. The IMP810 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}.

Low supply current makes the IMP809/IMP810 ideal for use in portable and battery operated equipment. The IMP809/IMP810 are available in a compact 3-pin SOT23 package.

Six voltage thresholds are available to support 3V to 5V systems:

Reset Threshold	
Suffix	Voltage (V)
L	4.63
M	4.38
J	4.00
T	3.08
S	2.93
R	2.63

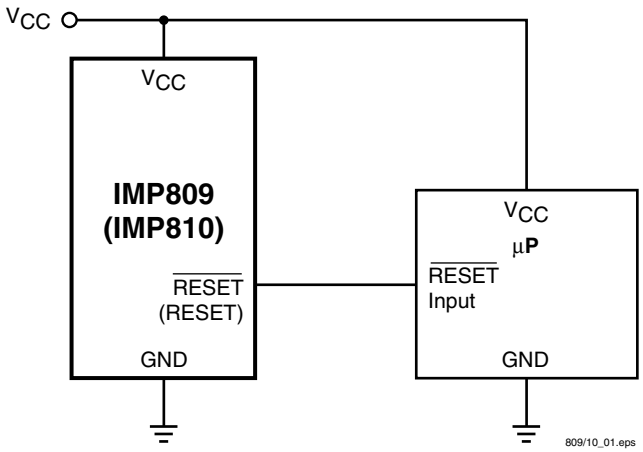
Key Features

- **Improved Maxim MAX809/MAX810 replacement**
  - **Lower supply current...6µA**
  - **80% lower maximum supply current**
- **Monitor 5V, 3.3V and 3V supplies**
- **140ms min. reset pulse width**
- **Active-low reset valid with 1.1V supply (IMP809)**
- **Small 3-pin SOT-23 package**
- **No external components**
- **Specified over full temperature range**
  - **–40°C to 105°C**

Applications

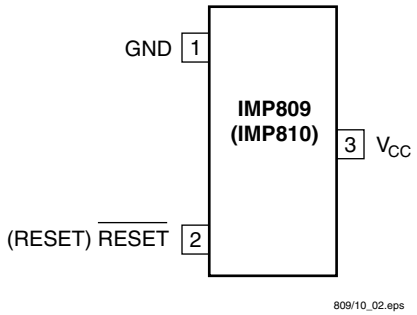
- Embedded controllers
- Battery operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment

Block Diagrams



Pin Configuration

SOT23



Ordering Information

Part Number [1]	Reset Threshold (V)	Temperature Range	Pin-Package	Package Marking[2] (XX Lot Code)
IMP809 Active LOW Reset				
IMP809LEUR-T	4.63	−40°C to +105°C	3-SOT23	AAXX
IMP809MEUR-T	4.38	−40°C to +105°C	3-SOT23	ABXX
IMP809JEUR-T	4.00	−40°C to +105°C	3-SOT23	CWXX
IMP809TEUR-T	3.08	−40°C to +105°C	3-SOT23	ACXX
IMP809SEUR-T	2.93	−40°C to +105°C	3-SOT23	ADXX
IMP809REUR-T	2.63	−40°C to +105°C	3-SOT23	AFXX
IMP810 Active HIGH Reset				
IMP810LEUR-T	4.63	−40°C to +105°C	3-SOT23	AGXX
IMP810MEUR-T	4.38	−40°C to +105°C	3-SOT23	AHXX
IMP810JEUR-T	4.00	−40°C to +105°C	3-SOT23	AIXX
IMP810TEUR-T	3.08	−40°C to +105°C	3-SOT23	AJXX
IMP810SEUR-T	2.93	−40°C to +105°C	3-SOT23	AKXX
IMP810REUR-T	2.63	−40°C to +105°C	3-SOT23	ALXX

Notes: 1. Tape and Reel packaging is indicated by the -T designation.
2. Devices may also be marked with full part number: 809L, 810M etc. XX refers to lot.

Related Products

	IMP809	IMP810	IMP811	IMP812
Max. Supply Current	15µA	15µA	15µA	15µA
Package Pins	3	3	4	4
Manual RESET input			■	■
Package Type	SOT-23	SOT-23	SOT-143	SOT-143
Active-HIGH RESET output		■		■
Active-LOW RESET output	■		■	

Absolute Maximum Ratings

Pin Terminal Voltage with Respect to Ground

V_{CC} . . . . . −0.3V to 6.0V
RESET, $\overline{RESET}$ . . . . . −0.3V to (V_{CC} + 0.3V)
Input Current at V_{CC} 20mA
Output Current: RESET, $\overline{RESET}$ 20mA
Rate of Rise at V_{CC} 100V/µs

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability

Power Dissipation (T_A = 70°C) 320mW
(Derate 4mW/°C above 70°C)
Operating Temperature Range . . . . . −40°C to 105°C
Storage Temperature Range . . . . . −65°C to 160°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

Electrical Characteristics

Unless otherwise noted V_{CC} is over the full voltage range, T_A = −40°C to 105°C.
Typical values at T_A = 25°C, V_{CC} = 5V for L/M/J devices, V_{CC} = 3.3V for T/S devices and V_{CC} = 3V for R devices.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input Voltage (V_{CC}) Range	V_{CC}	T_A = 0°C to 70°C T_A = −40°C to 105°C		1.1 1.2		5.5 5.5	V
Supply Current	I_{CC}	T_A = −40°C to 85°C T_A = −40°C to 85°C T_A = 85°C to 105°C T_A = 85°C to 105°C	V_{CC} < 5.5V, L/M/J V_{CC} < 3.6V, R/S/T V_{CC} < 5.5V, L/M/J V_{CC} < 3.6V, R/S/T		9 6	15 10 25 20	µA
Reset Threshold	V_{TH}	L devices	T_A = 25°C T_A = −40°C to 85°C T_A = 85°C to 105°C	4.56 4.50 4.40	4.63	4.70 4.75 4.86	V
		M devices	T_A = 25°C T_A = −40°C to 85°C T_A = 85°C to 105°C	4.31 4.25 4.16	4.38	4.45 4.50 4.56	
		J devices	T_A = 25°C T_A = −40°C to 85°C T_A = 85°C to 105°C	3.93 3.89 3.80	4.00	4.06 4.10 4.20	
		T devices	T_A = 25°C T_A = −40°C to 85°C T_A = 85°C to 105°C	3.04 3.00 2.92	3.08	3.11 3.15 3.23	
		S devices	T_A = 25°C T_A = −40°C to 85°C T_A = 85°C to 105°C	2.89 2.85 2.78	2.93	2.96 3.00 3.08	
		R devices	T_A = 25°C T_A = −40°C to 85°C T_A = 85°C to 105°C	2.59 2.55 2.50	2.63	2.66 2.70 2.76	
Reset Threshold Stability					30		ppm/°C
V_{CC} to Reset Delay		V_{CC} = V_{TH} to V_{TH} - 100mV			20		µs
Reset Active Timeout Period		T_A = −40°C to 85°C		140	240	560	ms
		T_A = 85°C to 105°C		100		840	
Low $\overline{RESET}$ Output Voltage (IMP809)	V_{OL}	V_{CC} = V_{TH} min., I_{SINK} = 1.2mA, IMP809R/S/T				0.3	V
		V_{CC} = V_{TH} min., I_{SINK} = 3.2mA, IMP809L/M/J				0.4	
		V_{CC} > 1.1V, I_{SINK} = 50µA				0.3	
High $\overline{RESET}$ Output Voltage (IMP809)	V_{OH}	V_{CC} > V_{TH} max., I_{SOURCE} = 500µA, IMP809R/S/T		0.8V_{CC}			V
		V_{CC} > V_{TH} max., I_{SOURCE} = 800µA, IMP809L/M/J		V_{CC} -1.5			
Low RESET Output Voltage (IMP810)	V_{OL}	V_{CC} = V_{TH} max., I_{SINK} = 1.2mA, IMP810R/S/T				0.3	V
		V_{CC} = V_{TH} max., I_{SINK} = 3.2mA, IMP810L/M/J				0.4	
High RESET Output Voltage (IMP810)	V_{OH}	1.8V < V_{CC} < V_{TH} min., I_{SOURCE} = 150µA		0.8V_{CC}			V

Notes: *1. Production testing done at T_A = 25°C. Over-temperature specifications guaranteed by design only.*
2. $\overline{RESET}$ output is active LOW for the IMP809 and RESET output is active HIGH for the IMP810

Pin Descriptions

Pin Number	Name	Function
1	GND	Ground
2 (IMP809)	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is asserted LOW if V_{CC} falls below the reset threshold and remains LOW for the 240ms typical reset timeout period (140ms minimum) after V_{CC} exceeds the threshold.
2 (IMP810)	RESET	RESET is asserted HIGH if V_{CC} falls below the reset threshold and remains HIGH for the 240ms typical reset timeout period (140ms minimum) after V_{CC} exceeds the threshold.
3	V_{CC}	Power supply input voltage (3.0V, 3.3V, 5.0V)

Detailed Descriptions

Reset Timing

The reset signal is asserted–LOW for the IMP809 and HIGH for the IMP810–when the V_{CC} signal falls below the threshold trip voltage and remains asserted for 140ms minimum after the V_{CC} has risen above the threshold.

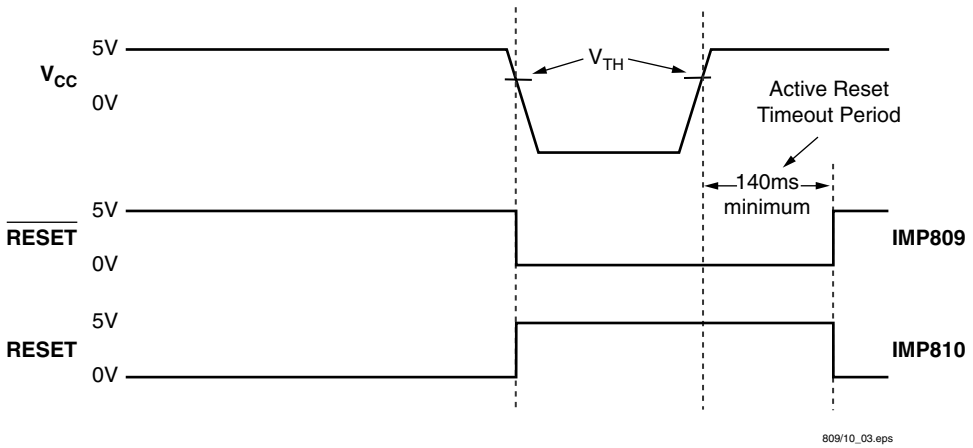


Figure 1. Reset Timing Diagram

Negative V_{CC} Transients

The IMP809/810 protect µPs from brownouts and low V_{CC}. Short duration transients of 100mV amplitude and 20µs or less duration typically do not cause a false RESET.

Valid Reset with V_{CC} under 1.1V

To ensure logic inputs connected to the IMP809 $\overline{\text{RESET}}$ pin are in a known state when V_{CC} is under 1.1V, a 100kΩ pull-down resistor at $\overline{\text{RESET}}$ is needed. The value is not critical. A pull-up resistor to V_{CC} is needed with the IMP810.

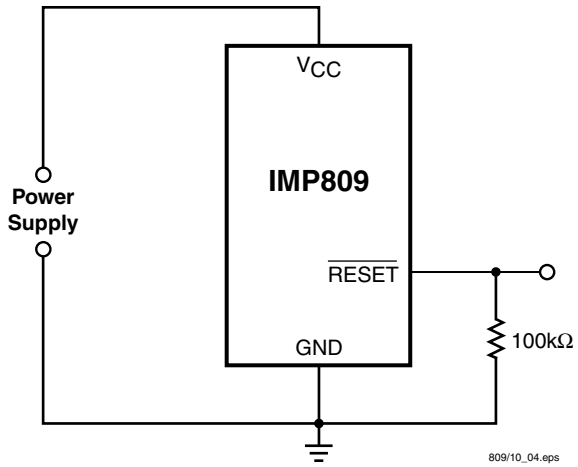


Figure 2. $\overline{\text{RESET}}$ Valid with V_{CC} Under 1.1V

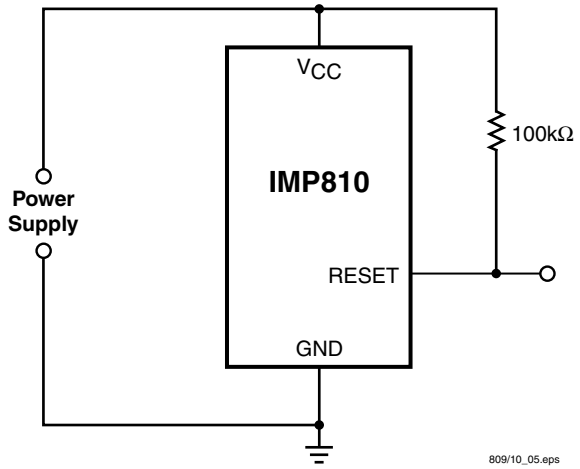


Figure 3. RESET Valid with V_{CC} Under 1.1V

Bi-directional Reset Pin Interfacing

The IMP809/810 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the IMP809/810 reset output and the µP/µC bi-directional reset pin.

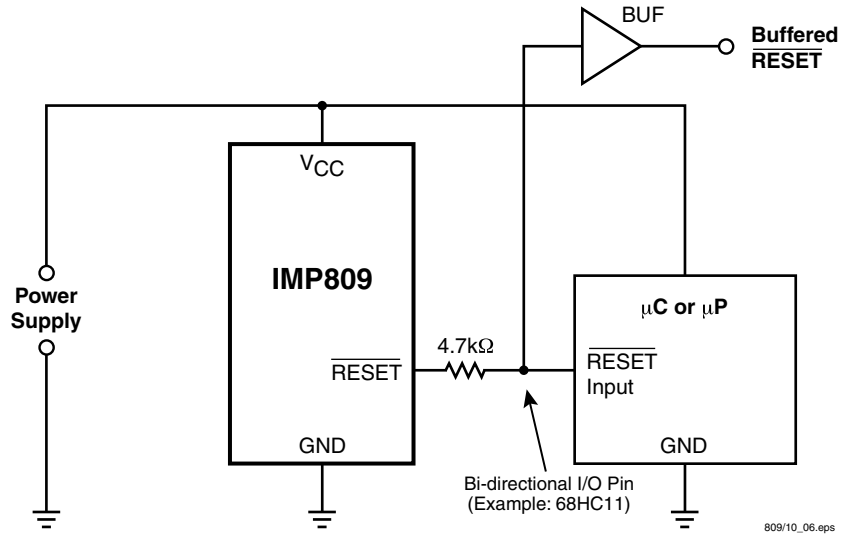
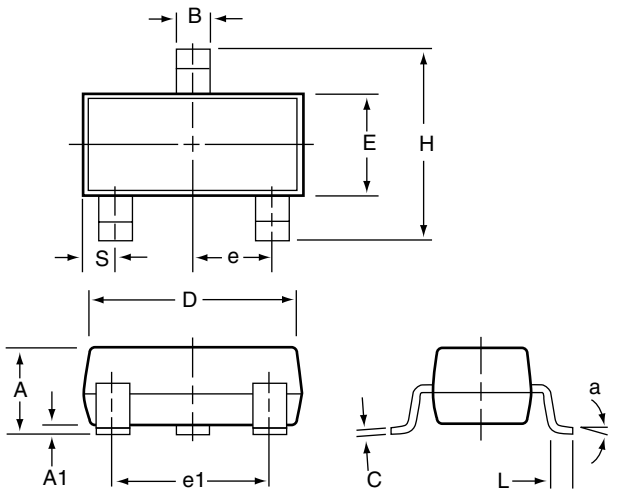


Figure 4. Bi-directional Reset Pin Interfacing

Package Dimensions

Plastic SOT-23 (3-Pin)



SOT-23 (3-Pin).eps

	Inches		Millimeters	
	Min	Max	Min	Max
Plastic SOT-23 (3-Pin)				
A	0.031	0.050	0.80	1.27
A1	0.004	0.010	0.10	0.25
B	0.015	0.020	0.37	0.51
C	0.003	0.007	0.085	0.18
D	0.110	0.120	2.80	3.04
E	0.047	0.055	1.20	1.40
e	0.035	0.040	0.89	1.03
e1	0.070	0.080	1.78	2.05
H	0.083	0.1039	2.10	2.64
L	0.027 REF		0.069 REF	
S	0.018	0.024	0.45	0.60

4-Pin µP Voltage Supervisor with Manual Reset

The IMP811/IMP812 are low-power supervisors designed to monitor voltage levels of 3.0V, 3.3V and 5.0V power supplies in low-power microprocessor (µP), microcontroller (µC) and digital systems. Each features a debounced manual reset input. The IMP811/812 are improved drop-in replacements for the Maxim MAX811/812 with extended temperature specifications to 105°C.

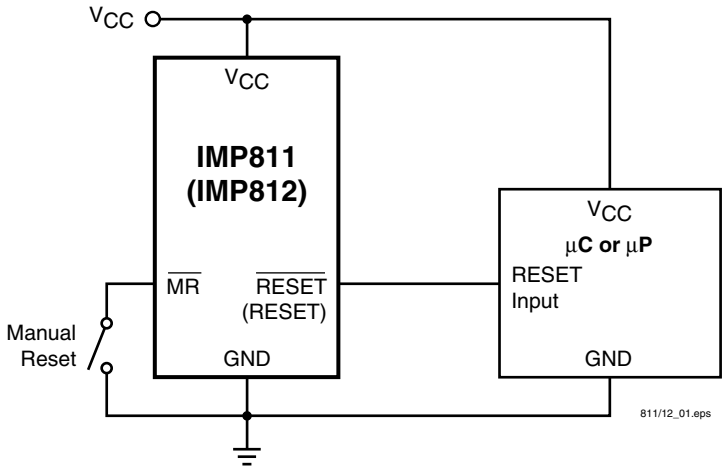
A reset signal is issued if the power supply voltage drops below a preset threshold and is asserted for at least 140ms after the supply has risen above the reset threshold. The IMP811 has an active-low output $\overline{\text{RESET}}$ that is guaranteed to be in the correct state for V_{CC} down to 1.1V. The IMP812 has an active-high output RESET. The reset comparator is designed to ignore fast transients on V_{CC} .

Low power consumption makes the IMP811/IMP812 ideal for use in portable and battery-operated equipment. Available in a compact 4-pin SOT143 package, the devices use minimal board space.

Six voltage thresholds are available to support 3V to 5V systems:

Reset Threshold	
Suffix	Voltage (V)
L	4.63
M	4.38
J	4.00
T	3.08
S	2.93
R	2.63

Block Diagrams



Key Features

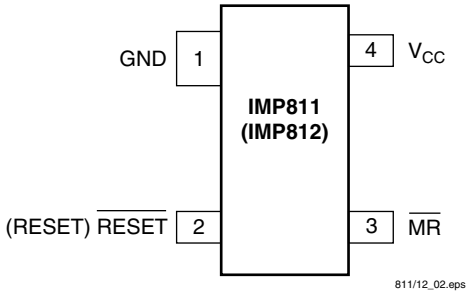
- Improved Maxim MAX811/MAX812 replacement
  - Specified to 105°C
  - New 4.0V threshold option
- 6µA supply current
- Monitor 5V, 3.3V and 3V supplies
- Manual reset input
- 140ms min. reset pulse width
- Guaranteed over temperature
- Active-LOW reset valid with 1.1V supply (IMP811)
- Small 4-pin SOT-143 package
- No external components
- Power-supply transient-immune design

Applications

- Computers and controllers
- Embedded controllers
- Battery operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment

Pin Configuration

SOT143



Ordering Information

Part Number [1]	Reset Threshold (V)	Temperature Range	Pin-Package	Package Marking[2] (XX Lot Code)
IMP811 Active LOW Reset with Active LOW Manual Reset				
IMP811LEUS-T	4.63	–40°C to +105°C	4-SOT143	AMXX
IMP811MEUS-T	4.38	–40°C to +105°C	4-SOT143	ANXX
IMP811JEUS-T	4.00	–40°C to +105°C	4-SOT143	AOXX
IMP811TEUS-T	3.08	–40°C to +105°C	4-SOT143	APXX
IMP811SEUS-T	2.93	–40°C to +105°C	4-SOT143	AQXX
IMP811REUS-T	2.63	–40°C to +105°C	4-SOT143	ARXX
IMP812 Active HIGH Reset with Active LOW Manual Reset				
IMP812LEUS-T	4.63	–40°C to +105°C	4-SOT143	ASXX
IMP812MEUS-T	4.38	–40°C to +105°C	4-SOT143	ATXX
IMP812JEUS-T	4.00	–40°C to +105°C	4-SOT143	AUXX
IMP812TEUS-T	3.08	–40°C to +105°C	4-SOT143	AVXX
IMP812SEUS-T	2.93	–40°C to +105°C	4-SOT143	AWXX
IMP812REUS-T	2.63	–40°C to +105°C	4-SOT143	AXXX

Notes: *1. Tape and Reel packaging is indicated by the -T designation.*
2. Devices may also be marked with full part number: 811L, 812M etc. XX refers to lot.

Absolute Maximum Ratings

Pin Terminal Voltage with Respect to Ground

V_{CC} . . . . . –0.3V to 6.0V
RESET, $\overline{\text{RESET}}$ and $\overline{\text{MR}}$ . . . . . –0.3V to (V_{CC} + 0.3V)
Input Current at V_{CC} and $\overline{\text{MR}}$ 20mA
Output Current: RESET or $\overline{\text{RESET}}$ 20mA
Rate of Rise at V_{CC} 100V/µs

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability

Power Dissipation (T_A = 70°C) 320mW
(Derate SOT-143 4mW/°C above 70°C)
Operating Temperature Range . . . . . –40°C to 105°C
Storage Temperature Range . . . . . –65°C to 160°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

Electrical Characteristics

Unless otherwise noted V_{CC} is over the full voltage range, T_A = –40°C to 105°C.
Typical values at T_A = 25°C, V_{CC} = 5V for L/M/J devices, V_{CC} = 3.3V for T/S devices and V_{CC} = 3V for R devices.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input Voltage (V_{CC}) Range	V_{CC}	T_A = 0°C to 70°C T_A = –40°C to 105°C		1.1 1.2		5.5 5.5	V
Supply Current (Unloaded)	I_{CC}	T_A = –40°C to 85°C T_A = –40°C to 85°C T_A = 85°C to 105°C T_A = 85°C to 105°C	V_{CC} < 5.5V, L/M/J V_{CC} < 3.6V, R/S/T V_{CC} < 5.5V, L/M/J V_{CC} < 3.6V, R/S/T		6 5	15 10 25 20	µA
Reset Threshold	V_{TH}	L devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	4.56 4.50 4.40	4.63	4.70 4.75 4.86	V
		M devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	4.31 4.25 4.16	4.38	4.45 4.50 4.56	
		J devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	3.93 3.89 3.80	4.00	4.06 4.10 4.20	
		T devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	3.04 3.00 2.92	3.08	3.11 3.15 3.23	
		S devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	2.89 2.85 2.78	2.93	2.96 3.00 3.08	
		R devices	T_A = 25°C T_A = –40°C to 85°C T_A = 85°C to 105°C	2.59 2.55 2.50	2.63	2.66 2.70 2.76	
Reset Threshold Temp. Coefficient	TC_{VTH}				30		ppm/°C
V_{CC} to Reset Delay		V_{CC} = V_{TH} to (V_{TH} - 125mV), L/M/J devices			40		µs
		V_{CC} = V_{TH} to (V_{TH} - 125mV), R/S/T devices			20		
Reset Active Timeout Period		T_A = 0°C to 70°C		140		560	ms
		T_A = –40°C to 105°C		100		840	
$\overline{MR}$ Minimum Pulse Width	t_{MR}			10			µs
$\overline{MR}$ Glitch Immunity		Note 3			100		ns
$\overline{MR}$ to RESET Propagation Delay	t_{MD}	Note 2			0.5		µs
$\overline{MR}$ Input Threshold	V_{IH}	V_{CC} > $V_{TH\ (MAX)}$, IMP811/812L/M/J		2.3			V
	V_{IL}					0.8	
	V_{IH}	V_{CC} > $V_{TH\ (MAX)}$, IMP811/812R/S/T		0.7V_{CC}			
	V_{IL}					0.25V_{CC}	
$\overline{MR}$ Pull-up Resistance				10	20	30	kΩ
Low $\overline{RESET}$ Output Voltage (IMP811)	V_{OL}	V_{CC} = V_{TH} min., I_{SINK} = 1.2mA, IMP811R/S/T				0.3	V
		V_{CC} = V_{TH} min., I_{SINK} = 3.2mA, IMP811L/M/J				0.4	
		V_{CC} > 1.1V, I_{SINK} = 50µA				0.3	
High $\overline{RESET}$ Output Voltage (IMP811)	V_{OH}	V_{CC} > V_{TH} max., I_{SOURCE} = 500µA, IMP811R/S/T		0.8V_{CC}			V
		V_{CC} > V_{TH} max., I_{SOURCE} = 800µA, IMP811L/M/J		V_{CC} -1.5			
Low RESET Output Voltage (IMP812)	V_{OL}	V_{CC} = V_{TH} max., I_{SINK} = 1.2mA, IMP812R/S/T				0.3	V
		V_{CC} = V_{TH} max., I_{SINK} = 3.2mA, IMP812L/M/J				0.4	
High RESET Output Voltage (IMP812)	V_{OH}	1.8V < V_{CC} < V_{TH} min., I_{SOURCE} = 150µA		0.8V_{CC}			V

Notes: *1. Production testing done at T_A = 25°C. Over temperature specifications guaranteed by design only using six sigma design limits.*
2. $\overline{RESET}$ output is active LOW for the IMP811 and RESET output is active HIGH for the IMP812.
3. Glitches of 100ns or less typically will not generate a reset pulse.

Pin Descriptions

Pin Number	Name	Function
1	GND	Ground
2 (IMP811)	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is asserted LOW if V_{CC} falls below the reset threshold and remains LOW for the 140ms minimum after the reset conditions are removed. In addition, $\overline{\text{RESET}}$ is active LOW as long as the manual reset is low.
2 (IMP812)	RESET	RESET is asserted HIGH if V_{CC} falls below the reset threshold and remains HIGH for the 140ms minimum after the reset conditions are removed. In addition, RESET is active HIGH as long as the manual reset is low.
3	$\overline{\text{MR}}$	Manual Reset Input. A logic LOW on $\overline{\text{MR}}$ asserts RESET. RESET remains active as long as $\overline{\text{MR}}$ is LOW and for 180ms after $\overline{\text{MR}}$ returns HIGH. The active low input has an internal 20kΩ pull-up resistor. The input should be left open if not used. It can be driven by TTL or CMOS logic or shorted to ground by a switch..
4	V_{CC}	Power supply input voltage (3.0V, 3.3V, 5.0V)

Related Products

	IMP809	IMP810	IMP811	IMP812
Max. Supply Current	15µA	15µA	15µA	15µA
Package Pins	3	3	4	4
Manual RESET input			■	■
Package Type	SOT-23	SOT-23	SOT-143	SOT-143
Active-HIGH RESET output		■		■
Active-LOW RESET output	■		■	

Detailed Description

Reset Timing and Manual Reset ($\overline{MR}$)

The reset signal is asserted–LOW for the IMP811 and HIGH for the IMP812 – when the V_{CC} signal falls below the threshold trip voltage and remains asserted for 140ms minimum after the V_{CC} has risen above the threshold.

A logic low on $\overline{MR}$ asserts $\overline{RESET}$ LOW on the IMP811 and HIGH on the IMP812. $\overline{MR}$ is internally pulled high through a 20kΩ resistor and can be driven by TTL/CMOS gates or with open collector/drain outputs. $\overline{MR}$ can be left open if not used.

$\overline{MR}$ may be connected to a normally-open switch connected to ground without an external debounce circuit.

For added noise rejection, a 0.1µF capacitor from $\overline{MR}$ to Ground can be added.

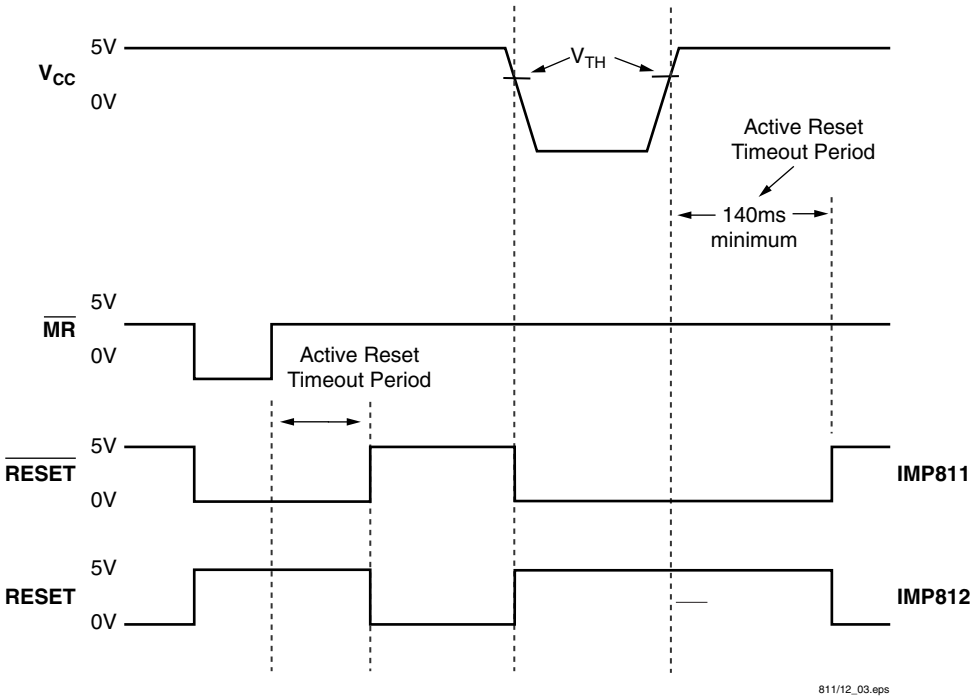


Figure 1. Reset Timing and Manual Reset (MR)

Application Information

RESET Output Operation

In µP/µC systems it is important to have the processor begin operation from a known state or be able to return the system to a known state. A RESET output to a processor is provided to prevent improper operation during power supply sequencing or low voltage – brownout – conditions.

The IMP811/812 are designed to monitor the system power supply voltages and issue a RESET signal when levels are out of range. RESET outputs are guaranteed to be active for V_{CC} above 1.1V. When V_{CC} exceeds the reset threshold, an internal timer keeps RESET active for the reset timeout period, after which RESET becomes inactive (HIGH for the IMP811 and LOW for the IMP812).

If V_{CC} drops below the reset threshold, RESET automatically becomes active. Alternatively, external circuitry or a human operator can initiate this condition using the Manual Reset ($\overline{MR}$) pin. There is an internal pullup on $\overline{MR}$ so it can be left open if it is not used. $\overline{MR}$ can be driven by TTL/CMOS logic or even an external switch, since it is already debounced. If the switch is at the end of a long cable, it might require a bypass (100nF) at the pin if noise pickup is a problem.

Six voltage thresholds are available to support 3V and 5V systems:

Reset Threshold	
Suffix	**Voltage (V)**
L	4.63
M	4.38
J	4.00
T	3.08
S	2.93
R	2.63

Valid Reset with V_{CC} under 1.1V

To ensure that logic inputs connected to the IMP811 $\overline{RESET}$ pin are in a known state when V_{CC} is under 1.1V, a 100kΩ pull-down resistor at $\overline{RESET}$ is needed. The value is not critical.

A similar pull-up resistor to V_{CC} is needed with the IMP812.

Negative V_{CC} Transients

Typically short duration transients of 100mV amplitude and 20µs duration do not cause a false RESET. A 0.1µF capacitor at V_{CC} increases transient immunity.

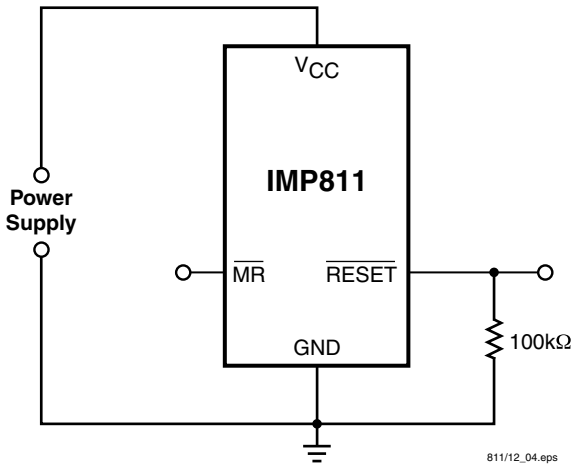


Figure 2. RESET Valid with V_{CC} Under 1.1V

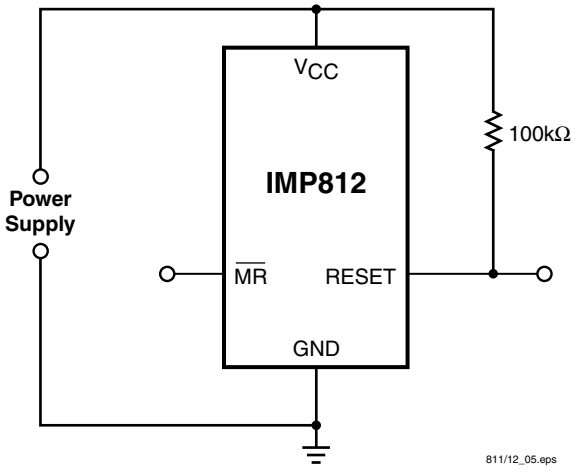


Figure 3. RESET Valid with V_{CC} Under 1.1V

Application Information

Bi-directional Reset Pin Interfacing

The IMP811/812 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the IMP809/810 reset output and the µP/µC bi-directional reset pin.

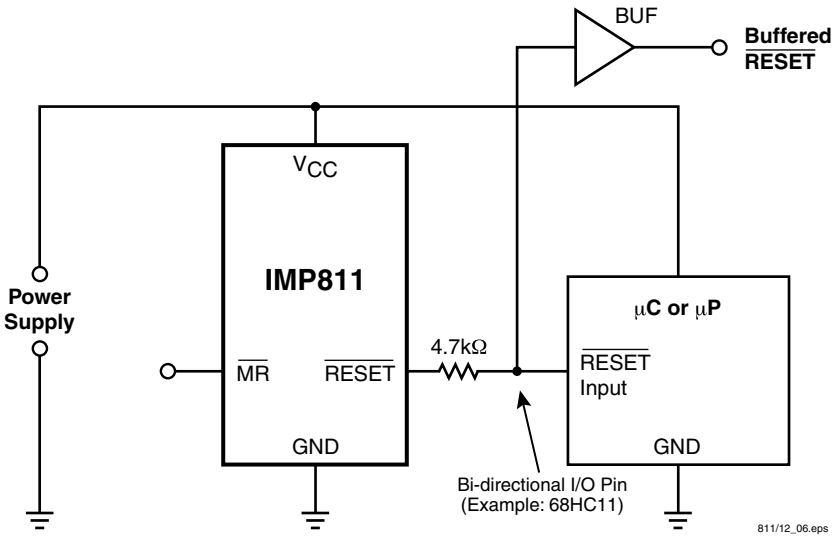
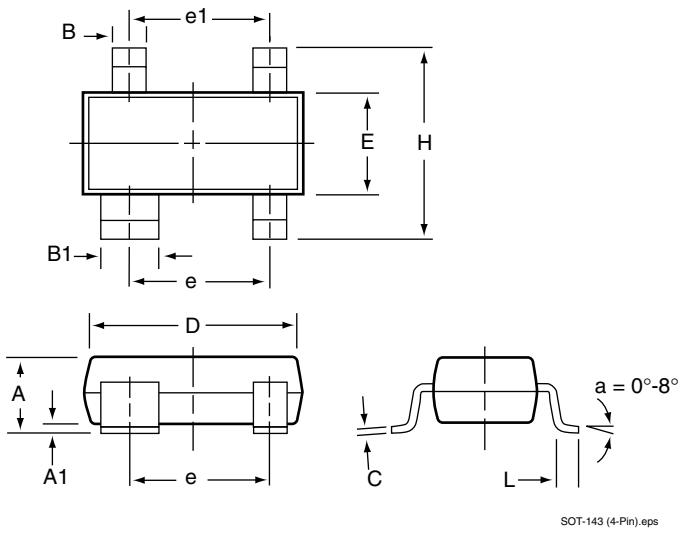


Figure 4. Bi-directional Reset Pin Interface

Package Dimensions

Plastic SOT-143 (4-Pin)



	Inches		Millimeters	
	Min	Max	Min	Max
Plastic SOT-143 (4-Pin)				
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
B1	0.030	0.038	0.762	0.965
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e	0.070	0.080	1.778	2.032
e1	0.071	0.079	1.803	2.007
H	0.082	0.098	2.083	2.489
I	0.004	0.012	0.102	0.305

IMP809, IMP810, IMP811, and IMP812L Maxim, and Analog Devices Part Numbers

The IMP809/810/811/812 supervisor family monitors the power supply of a microprocessor or microcontroller. When the monitored power supply voltage drops below the reset threshold, the supervisor chip generates a RESET signal for the system. The RESET signal is maintained active for a minimum time after the supply goes back above the reset threshold voltage.

Part Type	IMP Part Number	Maxim Part Number	Analog Device Part Number	Package Type	Reset Voltage (V)	Reset Output
809	IMP809LEUR	MAX809LEUR	ADM809LAR	3-pin SOT23	4.63 (L)	Active LOW
	IMP809MEUR	MAX809MEUR	ADM809MAR		4.38 (M)	
	IMP809JEUR	MAX809JEUR	ADM809JAR		4 00 (J)	
	IMP809TEUR	MAX809TEUR	ADM809TAR		3.08 (T)	
	IMP809SEUR	MAX809SEUR	ADM809SAR		2.93 (S)	
	IMP809REUR	MAX809REUR	ADM809RAR		2.63 (R)	
810	IMP810LEUR	MAX810LEUR	ADM810LAR	3-pin SOT23	4.63 (L)	Active HIGH
	IMP810MEUR	MAX810MEUR	ADM810MAR		4.38 (M)	
	IMP810JEUR	No equivalent	ADM810JAR		4.00 (J)	
	IMP810TEUR	MAX810TEUR	ADM810TAR		3.08 (T)	
	IMP810SEUR	MAX810SEUR	ADM810SAR		2.93 (S)	
	IMP810REUR	MAX810REUR	ADM810RAR		2.63 (R)	
811	IMP811LEUS	MAX811LEUS	ADM811LAR	4-pin SOT143	4.63 (L)	Active LOW
	IMP811MEUS	MAX811MEUS	ADM811MAR		4.38 (M)	
	IMP811JEUS	No equivalent	ADM811JAR		4.00 (J)	
	IMP811TEUS	MAX811TEUS	ADM811TAR		3.08 (T)	
	IMP811SEUS	MAX811SEUS	ADM811SAR		2.93 (S)	
	IMP811REUS	MAX811REUS	ADM811RAR		2.63 (R)	
812	IMP812LEUS	MAX812LEUS	ADM812LAR	4-pin SOT143	4.63 (L)	Active HIGH
	IMP812MEUS	MAX812MEUS	ADM812MAR		4.38 (M)	
	IMP812JEUS	No equivalent	ADM812JAR		4.00 (J)	
	IMP812TEUS	MAX812TEUS	ADM812TAR		3.08 (T)	
	IMP812SEUS	MAX812SEUS	ADM812SAR		2.93 (S)	
	IMP812REUS	MAX812REUS	ADM812RAR		2.63 (R)	

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408-432-9100/www.impweb.com

IMP705, IMP706, IMP707, IMP708 and IMP813L Maxim, Analog Devices and Sipex Part Numbers

Part Type	IMP Part Number	Maxim Part Number	Analog Device Part Number	Sipex Part Number	Package Type	Threshold Voltage
705	IMP705CPA	MAX705CPA	ADM705AN	SP705CP	8 pin, DIP	4.65V
	IMP705CSA	MAX705CSA	ADM705AR	SP705CN	8 pin, SO	4.65V
	IMP705CUA	MAX705CUA		SP705CU	8 pin, MicroSO	4.65V
	IMP705EPA	MAX705EPA	ADM705AN	SP705EP	8 pin, DIP	4.65V
	IMP705ESA	MAX705ESA	ADM705AR	SP705EN	8 pin, SO	4.65V
706	IMP706CPA	MAX706CPA	ADM706AN	SP706CP	8 pin, DIP	4.40V
	IMP706CSA	MAX706CSA	ADM706AR	SP706CN	8 pin, SO	4.40V
	IMP706CUA	MAX706CUA		SP706CU	8 pin, MicroSO	4.40V
	IMP706EPA	MAX706EPA	ADM706AN	SP706EP	8 pin, DIP	4.40V
	IMP706ESA	MAX706ESA	ADM706AR	SP706EN	8 pin, SO	4.40V
707	IMP707CPA	MAX707CPA	ADM707AN	SP707CP	8 pin, DIP	4.65V
	IMP707CSA	MAX707CSA	ADM707AR	SP707CN	8 pin, SO	4.65V
	IMP707CUA	MAX707CUA	ADM707ARM	SP707CU	8 pin, MicroSO	4.65V
	IMP707EPA	MAX707EPA	ADM707AN	SP707EP	8 pin, DIP	4.65V
	IMP707ESA	MAX707ESA	ADM707AR	SP707EN	8 pin, SO	4.65V
708	IMP708CPA	MAX708CPA	ADM708AN	SP708CP	8 pin, DIP	4.40V
	IMP708CSA	MAX708CSA	ADM708AR	SP708CN	8 pin, SO	4.40V
	IMP708CUA	MAX708CUA	ADM708ARM	SP708CU	8 pin, MicroSO	4.40V
	IMP708EPA	MAX708EPA	ADM708AN	SP708EP	8 pin, DIP	4.40V
	IMP708ESA	MAX708ESA	ADM708AR	SP708EN	8 pin, SO	4.40V
813L	IMP813LCPA	MAX813LCPA		SP813LCP	8 pin, DIP	4.65V
	IMP813LCSA	MAX813LCSA		SP813LCN	8 pin, SO	4.65V
	IMP813LCUA	MAX813LCUA		SP813LCU	8 pin, MicroSO	4.65V
	IMP813LEPA	MAX813LEPA		SP813LEP	8 pin, DIP	4.65V
	IMP813LESA	MAX813LESA		SP813LEN	8 pin, SO	4.65V

µPSuperXRef02

IMP690A, IMP692A, IMP812L, IMP812M, IMP805L Maxim, Analog Devices and Sipex Part Numbers

Part Type	IMP Part Number	Maxim Part Number	Analog Device Part Number	Sipex Part Number	Package Type	Threshold Voltage
690A	IMP690ACPA	MAX690ACPA	ADM690AAN	SP690ACP	8 pin, DIP	4.65V
	IMP690ACSA	MAX690ACSA	ADM690AARN	SP690ACS	8 pin, SO	4.65V
	IMP690AEPA	MAX690AEPA	ADM690AAN	SP690AEP	8 pin, DIP	4.65V
	IMP690AESA	MAX690AESA	ADM690AARN	SP690AES	8 pin, SO	4.65V
692A	IMP692ACPA	MAX692ACPA	ADM692AAN	SP692ACP	8 pin, DIP	4.40V
	IMP692ACSA	MAX692ACSA	ADM692AARN	SP692ACS	8 pin, SO	4.40V
	IMP692AEPA	MAX692AEPA	ADM692AAN	SP692AEP	8 pin, DIP	4.40V
	IMP692AESA	MAX692AESA	ADM692AARN	SP692AES	8 pin, SO	4.40V
802L	IMP802LCPA	MAX802LCPA	ADM802LAN		8 pin, DIP	4.65V
	IMP802LCSA	MAX802LCSA	ADM802LARN		8 pin, SO	4.65V
	IMP802LEPA	MAX802LEPA	ADM802LAN		8 pin, DIP	4.65V
	IMP802LESA	MAX802LESA	ADM802LARN		8 pin, SO	4.65V
802M	IMP802MCPA	MAX802MCPA	ADM802MAN		8 pin, DIP	4.40V
	IMP802MCSA	MAX802MCSA	ADM802MARN		8 pin, SO	4.40V
	IMP802MEPA	MAX802MEPA	ADM802MAN		8 pin, DIP	4.40V
	IMP802MESA	MAX802MESA	ADM802MARN		8 pin, SO	4.40V
805L	IMP805LCPA	MAX805LCPA	ADM805LAN		8 pin, DIP	4.40V
	IMP805LCSA	MAX805LCSA	ADM805LARN		8 pin, SO	4.40V
	IMP805LEPA	MAX805LEPA	ADM805LAN		8 pin, DIP	4.40V
	IMP805LESA	MAX805LESA	ADM805LARN		8 pin, SO	4.40V

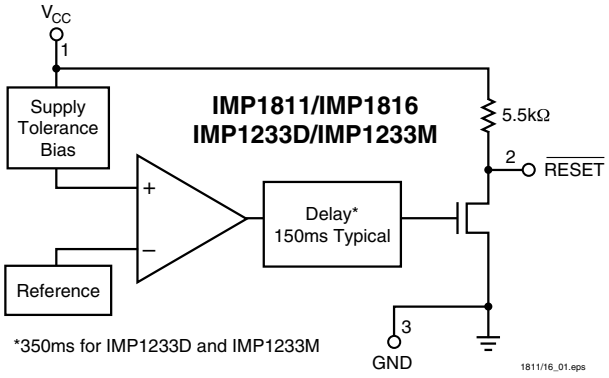
µPSuperXRef03

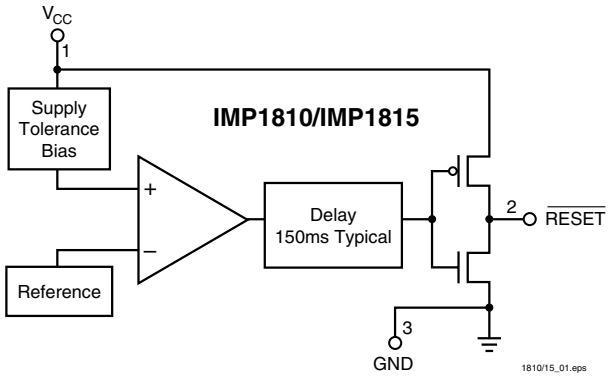
Low Power µP Supervisors

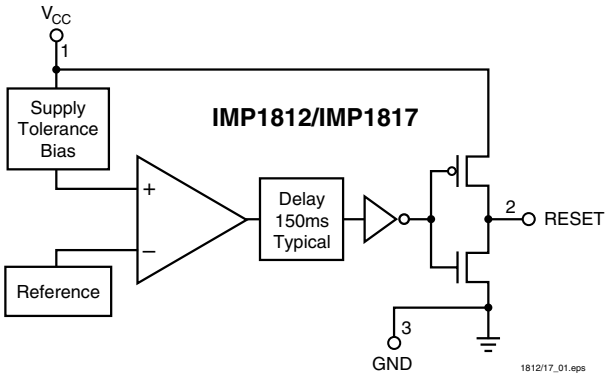
IMP offers pin compatible, lower-power versions of popular Dallas Semiconductor microprocessor supervisory circuits. For the latest information visit **www.impweb.com** or send specific requests to **info@impinc.com**.

Key Family Features

- Lower Power than Dallas Semiconductor Supervisors
  - 60% lower supply current
  - 15µA at 5.5V
  - 10µA at 3.6V
- Push-Pull and Open Drain Outputs
- Active LOW and Active HIGH Reset Options
- Compact TO-23 Surface Mount Package
- Two Reset Time Options: 150ms and 350ms
- Industrial Temperature Range







Family Selection Guide

Part	RESET Voltage (V)	RESET Time (ms)	Output Stage	RESET Polarity
IMP1810	4.620, 4.370, 4.120	150	Push-Pull	LOW
IMP1811	4.620, 4.370, 4.120	150	Open Drain	LOW
IMP1812	4.620, 4.350, 4.130	150	Push-Pull	HIGH
IMP1815	3.060, 2.880, 2.550	150	Push-Pull	LOW
IMP1816	3.060, 2.880, 2.550	150	Open Drain	LOW
IMP1817	3.060, 2.880, 2.550	150	Push-Pull	HIGH
IMP1223D	4.625, 4.375, 4.125	350	Open Drain	LOW
IMP1233M	4.625, 4.375, 2.720	350	Open Drain	LOW

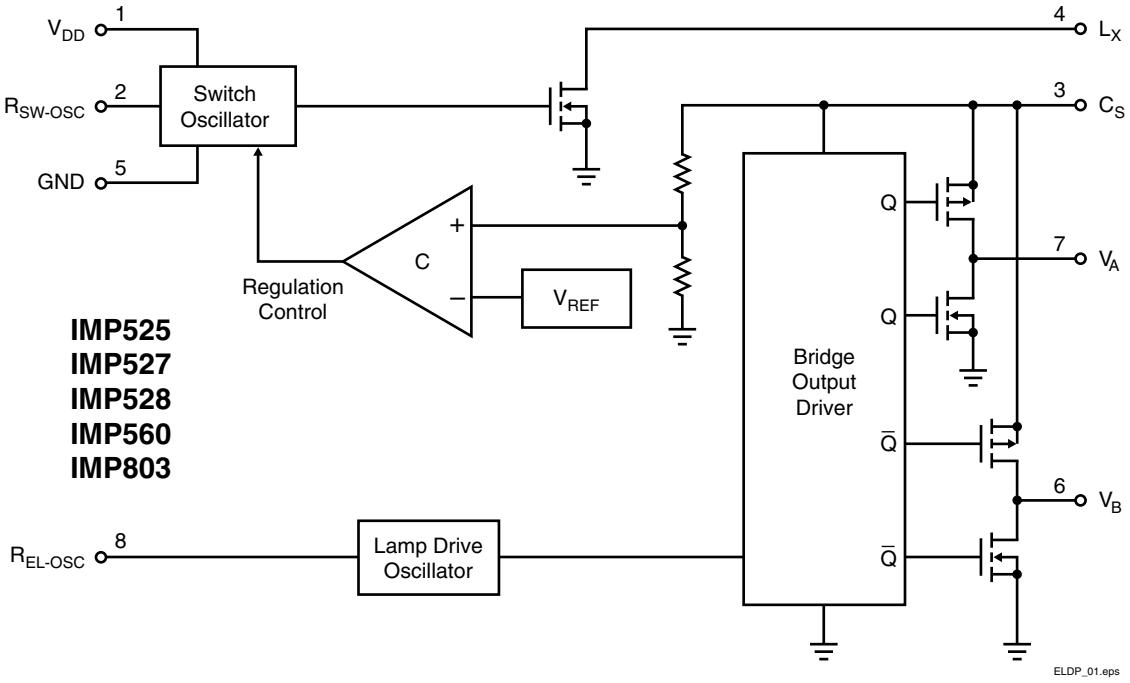
IMP Electroluminescent Lamp Drivers

IMP electroluminescent lamp drivers incorporate four EL lamp driving functions on-chip. These are the boost switch-mode power supply, its high-frequency oscillator, the high-voltage H-bridge lamp driver and its low-frequency oscillator. Few external components are needed: one inductor, one diode, one capacitor and two resistors. The resistors allow independent adjustment of boost converter frequency and of EL lamp drive frequency. Adjustable lamp drive frequency allows control over lamp color and power dissipation. All devices can be disabled for power savings.

All devices are available in chip form and small MicroSO and SO packages. Tape and reel shipment is available without additional cost.

Applications

- PDAs
- Safety illumination
- Portable instrumentation
- Battery-operated displays
- LCD modules
- Toys
- Automotive displays
- Cellular phones
- Night lights
- Audio and TV remote control units
- Panel meters
- Pagers
- Clocks and radios
- Portable GPS receivers
- Handheld computers
- Caller ID



EL Lamp Driver Product Summary Table

Part	Input Voltage Range (V)	Packages	Low Power Disable Mode	Typical Output Voltage (V_{PP})	Adjustable Lamp Drive and Boost Frequency	Regulated Output Voltage
IMP525	0.9 to 2.5	MicroSO & SO	Yes	112	Yes	Yes
IMP527	0.9 to 2.5	MicroSO & SO	Yes	180	Yes	Yes
IMP528	2 to 6.5	MicroSO & SO	Yes	220	Yes	Yes
IMP560	2 to 6	MicroSO & SO	Yes	120	Yes	Yes
IMP803	2 to 6	MicroSO & SO	Yes	180	Yes	Yes

All devices are available in die form.

ELDP_t01.eps

ISO 9001 Registered

IMP, Inc.
Corporate Headquarters
2830 N. First Street
San Jose, CA 95134-2071
Tel: 408-432-9100
Tel: 800-438-3722
Fax: 408-434-0335
e-mail: info@impinc.com
http://www.impweb.com

Publication #: 1010
Revision: B
Issue Date: 08/17/99
Type: Product